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Improvement in Performance of Induction Motor Drive Using Multilevel Inverter

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Abstract

As we know that in India, rate of energy generation is greater than that of the energy saving. So there is necessity of energy saving in India..And energy saving has more importance in present condition. Electric motor used about 70% generated energy in industrialized countries. And more than 60% of electric energy is converted in to mechanical energy is consumed by pump and drives. This facts out importance of energy saving in these types of drives In this paper we have given detail study about improvement in performance of induction motor using Multilevel Inverter.

Keywords*: Total Harmonic Distortion (THD) Common Mode Voltage(CMV), Induction Motor, Multilevel Inverter, Space Vector Pulse Width Modulation(SVPWM)*

I. Introduction

The main objective of this thesis is to design a system which minimizes total harmonic distortion, switching losses and to improve the performance of drive system. In conventional two-level inverter configuration, the harmonic reduction in output is achieved mainly by raising

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the switching frequency. But in high power applications, the switching frequency of the power device has to be restricted below 1 KHz due to the increased switching losses and also the level of dc-bus voltage. On the other hand, the very high dv/dt generated with high dc-link voltage is responsible for the electromagnetic interference and motor winding stress. So from the aspect of harmonic reduction and high dc-link voltage level, multi-level inverters are more suitable.

In case of two-level inverter, the blocking capacity can be increase by connecting the switching devices in series. A multilevel inverter can reduce as well as eliminate the CMV. Multilevel inverters have a high number of switching states so that the output voltage is stepped in smaller increments. This allows mitigation of the harmonics at low switching frequencies thereby reducing switching losses. Further, the leakage current is reduced because of the lower dv/dt. . So from the aspect of harmonic reduction and high dc-link voltage level, multi-level inverters are more suitable. Rate of energy generation is greater than that of the energy saving. So there is necessity of energy saving in India..And energy saving has more importance in present condition

In present condition energy saving is important. so there is necessity of energy saving in these type of drives. By using new SVPWM technique, the common mode voltage, harmonic distortion and improvement in the performance of drives.

II. Classification of Multilevel Inverter

Basic multilevel inverter can categorized in to three types.

- **Diode clamped (DCMI)**
- **Flying Capacitor(FCMI)**
- **Cascaded inverter.(CI)**

The DCMI uses capacitors in series to divide up the DC bus voltage in to a set of voltage. These inverters have high efficiency and method used is back to back inter tie system, And drawback is o use large clamping diode.

In FCMI, a ladder structure of DC side capacitor is used where the voltage on each capacitor is differs. In this case switching losses is very high, especially due to real power transfer.

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In CI, the DC sources are separated and this inverter can avoid extra clamping diode or voltage balancing capacitors.

2.1 Space vector pulse width modulation (SVPWM)

A Multilevel inverter are increasingly used in high power applications due to their superior performance compared with two level inverter, such as common mode voltage, lower dv/dt,lower harmonic distortion and improve in the performance of drive system .The advantage of this is ,it directly uses control variable given by control system.

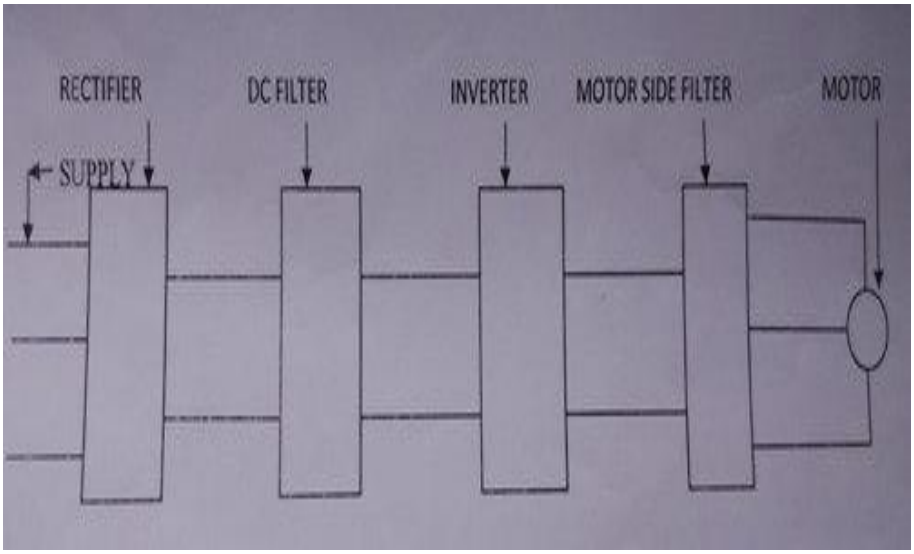

Fig .1. Diagram for Power electronic conversion system for induction motor

The space vector diagram of any three phase n level inverter consists of six sectors. Each sector consists of (n-1)2 triangles. The tip of reference vector can be located within any triangle…Each vertex represent switching vector. there are n^3 switching states in space diagram.

The SVPWM is performed by suitably selecting and executing the switching state of triangle for respective on time

The main objective of this thesis is to design a system which eliminate total harmonic distortion, switching losses and improve performance of drive system as compared with two level inverter. Recently the Multilevel Inverter has drawn tremendous interest in the power electronics industry.

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Multilevel inverters start from three-level. There are different types of multilevel inverters. In this work diode clamped multilevel inverter is used to drive three phase induction motor. This system may be used for medium voltage drive system.

A multilevel inverter can be used to reduce CMV, THD and to improve the performance of drive system. Multilevel inverter has a high number of switching states so that the output voltage step is in small increment. This allows migration of the harmonics at low switching frequencies thereby reducing switching losses. Further the leakage current is reduced because of lower dv/dt.

In multilevel inverters, it is easy to reach high voltage levels in high power applications with lower harmonic distortion and switching frequency, which is very difficult to get this performance with conventional two level inverter

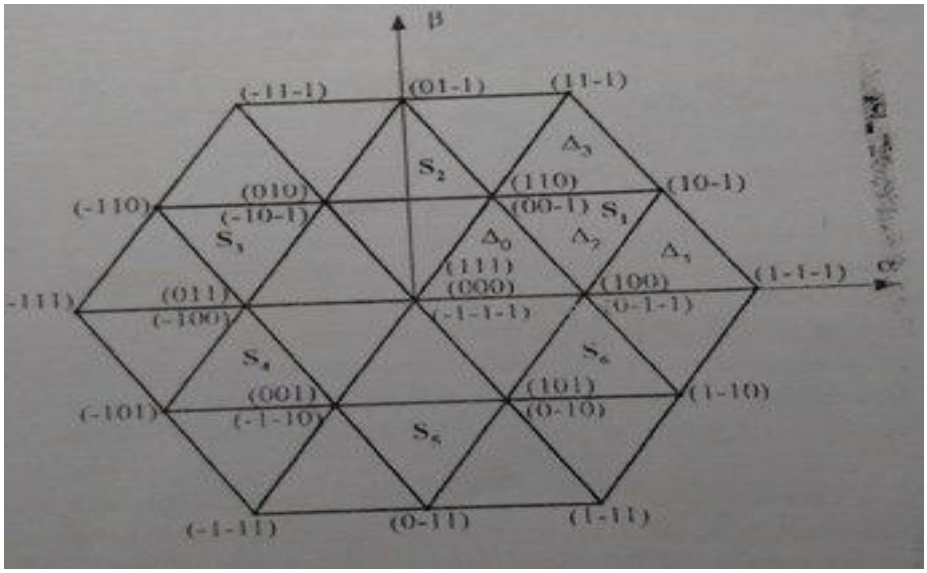

Fig .2. Space Vector Diagram for Three-Level inverter

A multi level space vector plane is transformed in to two level space vector plane by using two step.
(1) From the location of given reference voltage, one hexagon has to be selected
(2) Original reference vector has to be subtracted by the amount of center voltage vector.

Determination of switching sequence and calculation of voltage vector duration time is done in conventional two level SVPWM method.

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The two level inverter contain more losses as compared with three level inverter. Like total harmonic distortion, common mode voltage, improvement in performance of drive system.

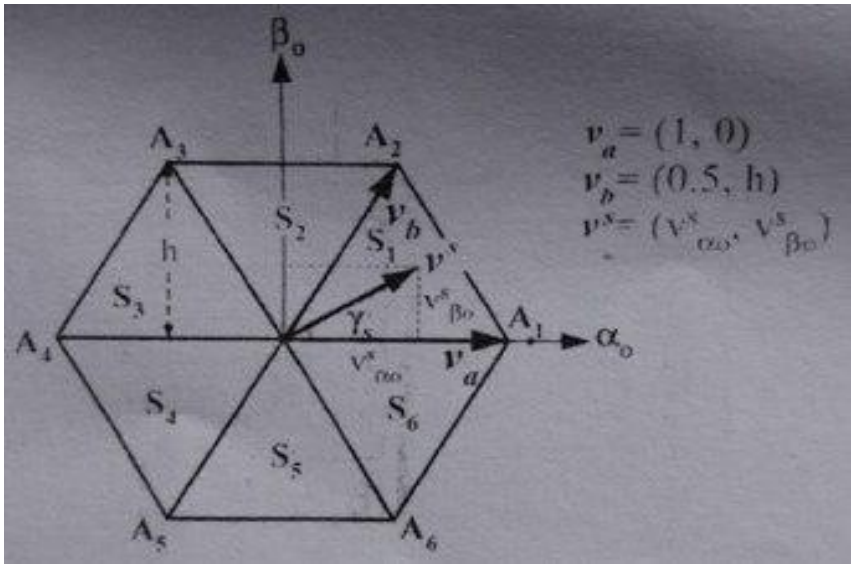

Fig.3. Space Vector Diagram for Two-Level inverter

Fig.2 shows the space vector diagram for three level inverter. Contain six vector (S1-S6) and four triangles in each sector .fig.3 shows the space vector diagram for two level inverter.

2.2 Common –Mode Voltage (CMV)

The CMV is defined as the voltage at star point of the load and the ground Magnitude depend upon the grounding system .The definition of CMV consist of well defined edges that are responsible for common mode current.

V com=1/3(Vag + Vbg + Vcg) Vdc =Vng
Since Vsi can not provide purely sinusoidal voltage and descrete output voltages synthesized fom dc bus voltageVdc.The CMv is always different from zero and take values of +Vdc/6 or +vdc/2.depending upon the inverter switch selected.uring the switch state changes,the CMv changes by +Vdc.The CMV transitions are shown in fig 4 The changes in CMV from –Vdc/2 to –Vdc/6 constitutes step of Vdc/3.When the level changes from –Vdc/6 to Vdc/6 .

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By using this modulation common mode converter must be reduced, however three level inverter present a good chance for zero sequence noise reduction.

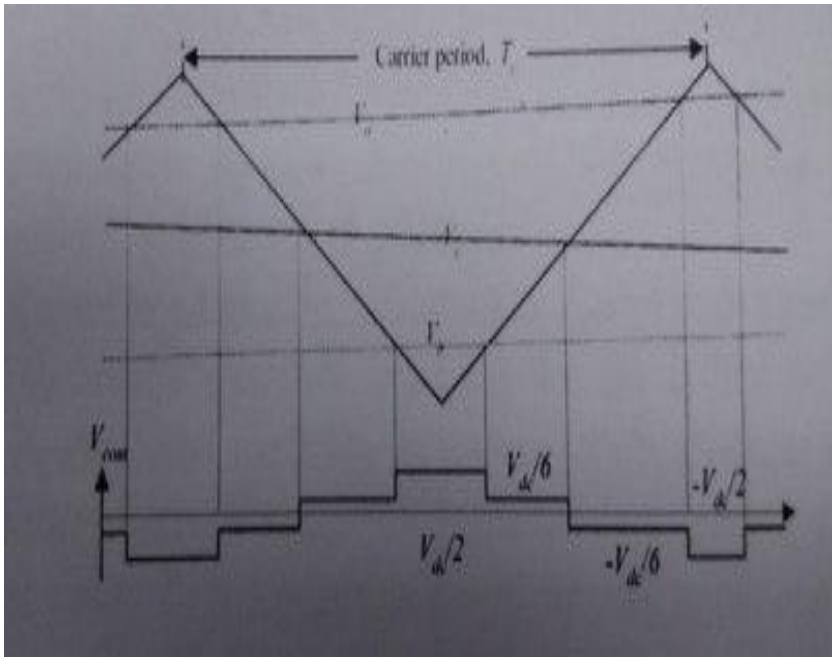

Fig.4. Reference Voltage Carrier Waveform And CMV when SPWM applied to two level inverter.

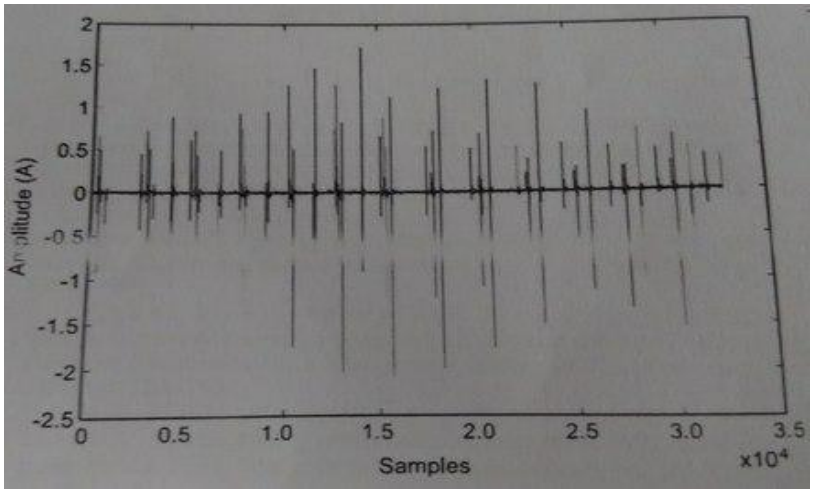

Fig.5. Common mode current spectra for two level inverter

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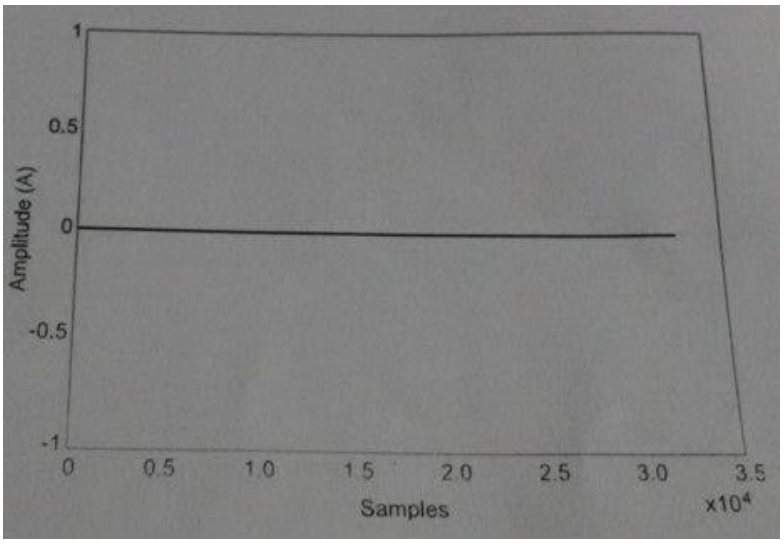

Fig.6. Common mode current spectra for three level inverter

From the Fig no.5 & 6, The common mode current spectra for two level and three level are compared. The common mode current are the main cause of bearing fault condition in induction motor drive. From the above diagram, we can say that, in three levels inverter fault are less than that of two level inverter.

The fig 7,8 are common mode voltage spectra for two and three level inverter. The common mode voltage on two level inverter has two different components, one of which lower amplitude a low frequency that is due to voltage oscillation on capacitors and second one is three times switching frequency with amplitude. The higher frequency is much critical because it causes common fault effect.

In two level, some noise components are obtained .and in three level ,noise level will be disappear.

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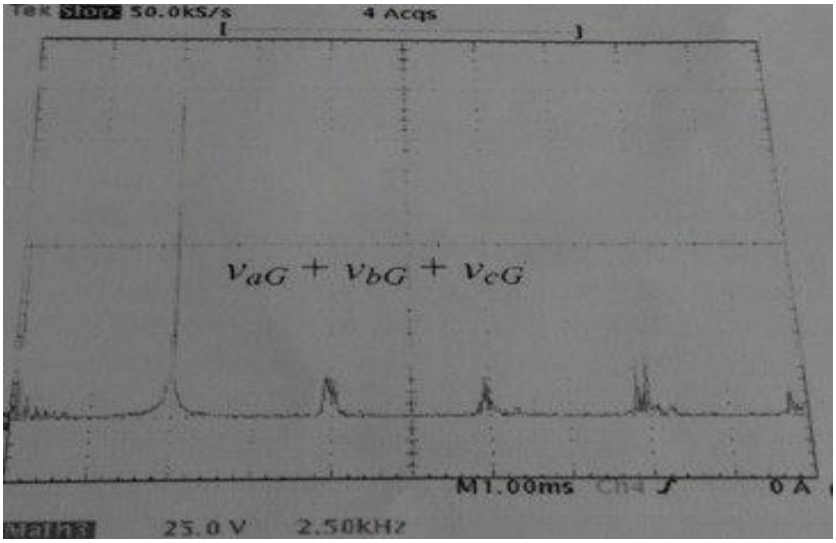

Fig.7. Common mode voltage spectra for two level inverter.

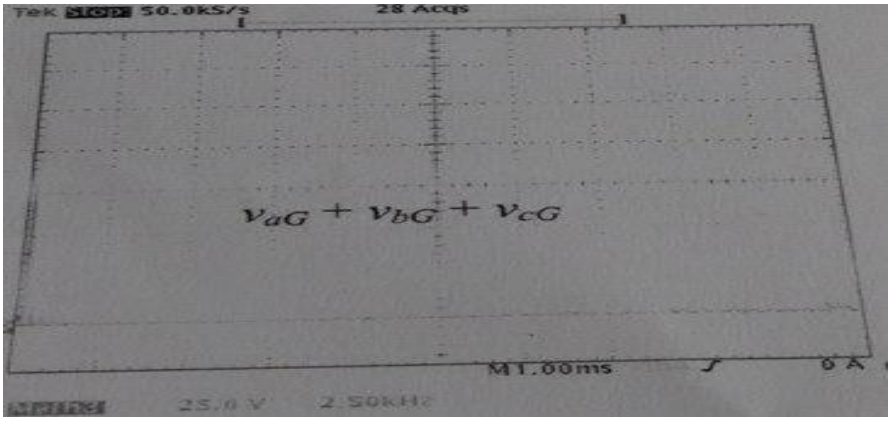

Fig.8. Common mode voltage spectra for three level inverter.

In fig.9, 10 the common mode voltage on time domain for two level and three level are to be compared.

The high frequency noise clearly shown in three level inverter. And demonstrates modulation efficiency on high frequency noise modulation.

Three level converter especially in case of diode clamping configuration allows introducing zero voltage sequence common mode modulation by using medium voltage…by these three level

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inverter, modulation effect can be reduced as compared with two level inverter. And three level converters present a good condition for zero noise sequence reduction that allows increasing induction motor life. Also In this case zero sequence noise reduction and common mode voltage will be disappear and machines life is increased.

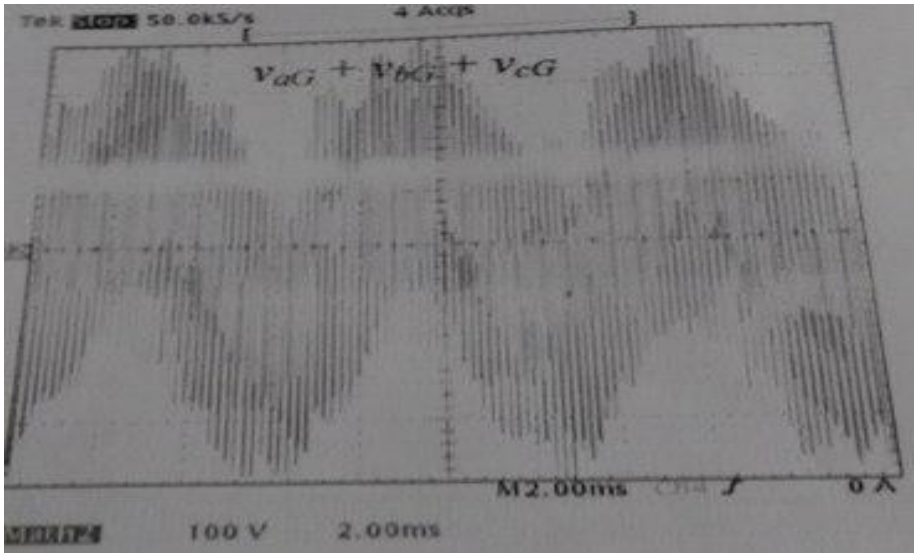

Fig.9. Common mode voltage on time domain for two level inverter.

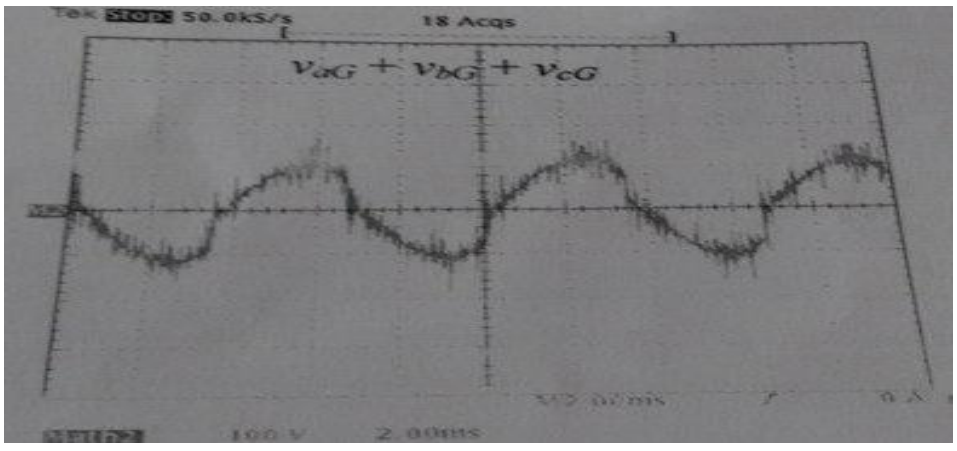

Fig.10. Common mode voltage on time domain for three level inverter.

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III. Conclusions

In various papers different methods are used to reduced, switching losses and minimum harmonic distortion and improve performance of drive system.

In case of two level inverter, the total harmonic distortion, switching losses is more as compared with multilevel inverter. Hence we used multilevel inverter to reduced the total harmonic distortion, switching losses.

In multilevel inverters, it is easy to reach high voltage levels in high power applications with lower harmonic distortion and switching frequency, which is very difficult to get this performance with conventional two level inverter.

Multi-level voltage source inverters offer several advantages such as a better output voltage with reduced total harmonic distortion (THD) the application of simplified space vector modulation (SVM) method for three-level diode clamped inverters feeding a Induction motor.

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