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AN ADVANCED STEP-UP SINGLE-PHASE FIVE-LEVEL INVERTER

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Abstract

In this paper, an enhanced step-up five-level inverter is proposed for photovoltaic systems. Compared with conventional five-level inverters, the proposed topology can realize the multilevel inversion with high step-up output voltage, simple structure, and reduced number of power switches. The operating principle of the proposed inverter has been analyzed and the output voltage expression has been derived. In addition, the comparison with existing topologies of single-phase five-level inverters is presented. Finally, simulation results validate the performance of the proposed topology.

Index Terms—Multilevel inverter, single phase, step up, switch-diode- capacitor cell.

I. INTRODUCTION

In the past decade, renewable energy sources such as photovoltaic (PV)-based systems have attracted much more attention due to the advantages such as less environmental impact and improved economic benefits. With the rapid growth of power electronics technology, various converters topologies have been developed for PV systems. Among these topologies, multilevel inverters have been receiving significant interest due to the reduced total harmonic distortion (THD) and improved quality of output waveform. As the output voltage level increases, the output harmonic content of such inverters decreases, allowing the use of smaller output filters.

For single-phase multilevel inverters, the most common topologies are the neutral-point clamped (NPC), flying capaci- tor (FC) and the cascaded H-bridges (CHB) types [2]–[5]. Some extended topologies for NPC have been further discussed in [6]– [8] and new topologies for the cascaded-type-based multilevel inverter have been proposed in [9]–[11]. In recent years, modu- lar multilevel converter (MMC) has become an attractive topol- ogy due to its modularity, inherent redundancy, improved power quality, and ease of expansion [12]. Nevertheless, the number of component MMC used is not reduced and two inductors are added. Alternatively, some multilevel topologies with coupled inductors are proposed in [13]–[16] and they increase the num- ber of output voltage levels without the need for a number of dc sources and bulky capacitors. The drawback is that coupled inductors need to be carefully designed.

Overall, the aforementioned multilevel topologies only can realize the voltage step-down inversion, i.e., the ac voltage amplitude cannot exceed the input dc voltage. A "transformerless" architecture is competent since it reduces the system cost and weight and realizes the voltage step up [17], [18]. However, two dc sources and corresponding split of dc bus capacitors are re- quired as well as more switches and diodes in [17]. The step-up ratio of the boost converter has some limitations which restrict the step-up capability [18]. A high step-up inverter is proposed in [19] using the diode–capacitor cell and couple inductor. It uses less switches but just implements the two-level inversion.

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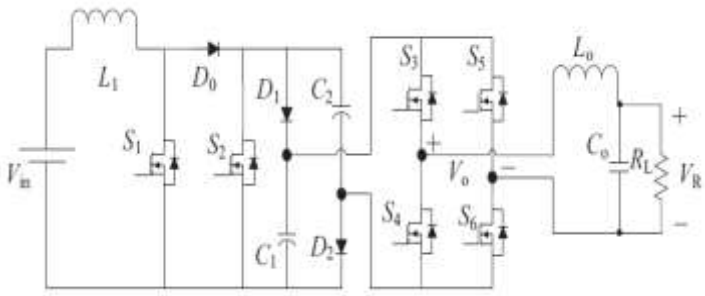


Fig. 1. Topology of the proposed -phase step-up five-level inverter.

In this paper, a novel single-phase step-up five-level inverter is proposed using the switch-diode-capacitor cell [20]. Com- pared to the conventional five-level topologies, the proposed inverter has the following advantages: 1) reduced number of power switches, diodes, and a single dc source are used; 2) mul- tilevel inversion with step-up output voltage is obtained; 3) only four switches work at high frequency while two switches work at low frequency (50 Hz), which helps to reduce the switching losses; 4) simple topology and easy control are achieved.

II. PROPOSED SINGLE-PHASE STEP-UP FIVE-LEVEL INVERTER

Fig. 1 shows the topology of the proposed single phase step-up five-level inverter. As shown in Fig. 1, it consists of a single dc source, a conventional boost converter, a switch- diode-capacitor cell, and an H-bridge. The diode–capacitor cell (C_1 –D_1 , C_2 –D_2) and the inductor L_1 are used to boost the dc- link voltage. The multilevel signal is generated by switch S_2 and the diode–capacitor cell. The proposed topology can implement the multilevel inversion with high step-up output voltage.

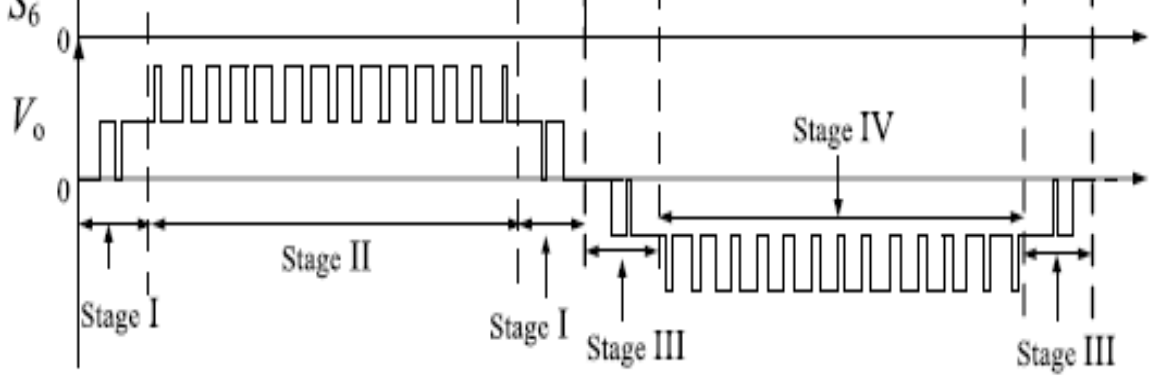
A. Modulation Method

As shown in Fig. 2, this proposed topology uses the level-shift multicarrier-based pulse width modulation method. Assuming that the capacitors C_1 and C_2 are equal and the diode–capacitor cell (C_1 –D_1 , C_2 –D_2) is symmetrical and balanced, one can obtain

$$C_1 = C_2 = C, \; u_{C1} = u_{C2} = U_C \qquad (1)$$

where u_{C1} and u_{C2} are the voltage across the capacitors

C_1 and C_2. The following analysis is also based on the assumption that the capacitor voltage is constant. Depend- ing on the intersections between the reference and carrier, it can be seen that two stages exist in positive reference wave (Stages I and II) and negative reference wave (Stages III and IV).



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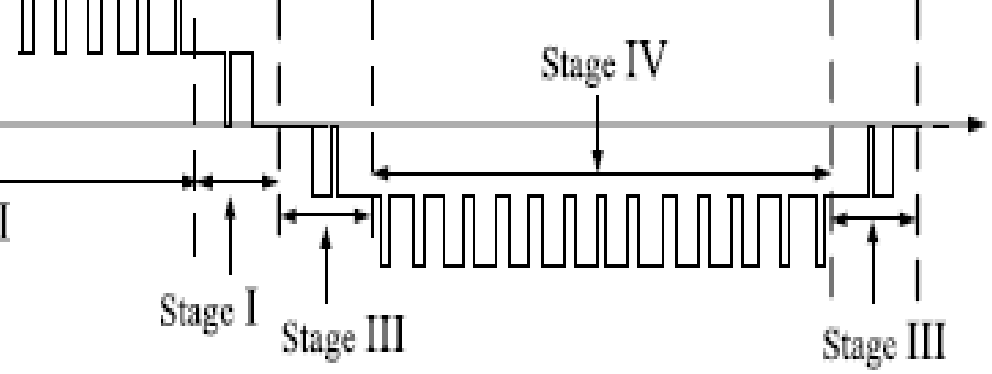

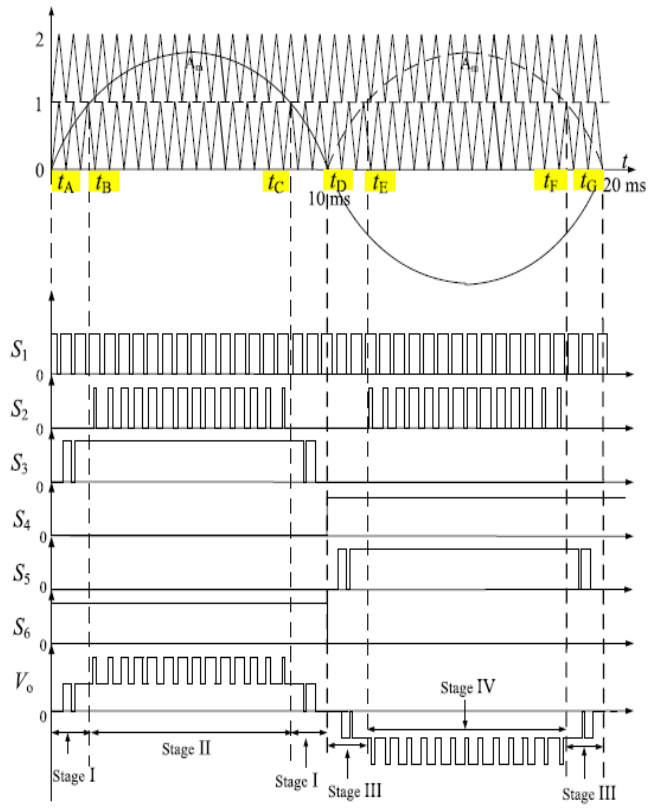

Fig. 2. Modulation method of the proposed step-up five-level inverter.

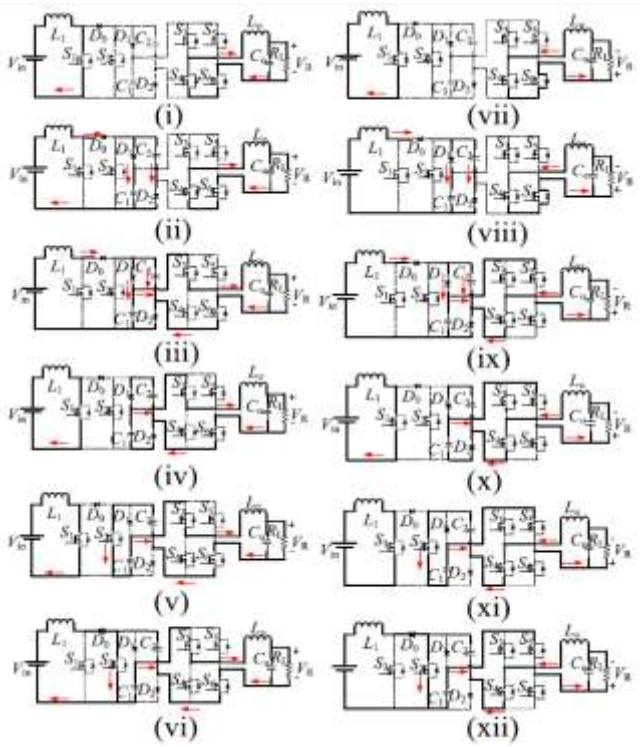

Fig. 3. Equivalent circuits of the proposed five-level inverter, (i)—(xii) modes

1) Positive Output Voltage (tA < t < tD):
Switches S4 and S5 are maintained OFF state in the positive output voltage period.

Stage I (tA < t < tB , tC < t < tD):
The switch S3 is switching due to the intersection between the sinusoidal reference waveform and the lower carrier waveform. In this stage, S2 is OFF while S6 is maintained ON state.

The modes 1–4 shown in Fig. 3(i)–(iv) work alternately and the output voltage of the inverter Vo is 0 or Uc .

Stage II (tB < t < tC):
The switch S2 is switching due to the intersection between the sinusoidal reference waveform and the upper carrier waveform. S3 is maintained ON state during this period. In Stage II, the modes 3– 6 shown in Fig. 3 (iii) and (vi) operate alternately and the output voltage of the inverter Vo is uc or 2Uc .

2) Negative Output Voltage (tD < t < tG):
When the output voltage is negative, switches S3 and S6 are maintained OFF state. Stages III and IV are the counterpart of Stages I and II in the negative output of the ac voltage, respectively.
The switching states and corresponding modes are summarized in Table I. Generally, the switches in the H-bridge (S3–S6) work to determine the polarity of the output voltage and switch S2 operates to determine the output voltage level.

Table I: Switching states and working modes

Stage	Switching states	Possible modes
I	S1 , S3 : switching, S2 , S4 , S5 : OFF, S6 : ON	Modes 1, 2, 3, 4
II	S1 , S2 : switching, S4 , S5 : OFF, S3 , S6 : ON	Modes 3, 4, 5, 6
III	S1 , S5 : switching, S2 , S3 , S6 : OFF, S4 : ON	Modes 7, 8, 9, 10
IV	S1 , S2 : switching, S3 , S6 : OFF, S4 , S5 : ON	Modes 9, 10, 11,12

B. Operating Principle
The below figures shows the working mode of the proposed five-level inverter. The red arrows in the figures show the current path.
Overall, it can be seen that there are six switching states in each half-cycle. The operating modes of the positive half sinusoidal cycle (modes 1–6) are discussed in detail as follows.

Mode 1:
S1 is turned ON in this mode. The inductor L1 is charged by the input dc source and the inductor current is increasing linearly. Meanwhile, the load current flows through S6 and anti parallel diode of S4.

Mode 2:
S1 is turned OFF in this mode. Diodes D0 , D1 , and D2 are all conducting. The inductor L1 is discharging

and the input source is charging the diode–capacitor network. In this mode, the ac load current still flows through S6 and anti parallel diode of S4

Mode 3:
S1 is maintained OFF and S3 is ON in this mode. Diodes D0 , D1 , and D2 are maintained ON. The input dc source charges the diode–capacitor cell and simultaneously provides the power to the load.

Mode 4: S1 is turned ON again while D0 is turned OFF in this mode. L1 is charged by the input source and capacitors C1 and C2 are working in parallel to feed the load.

Mode 5: S1 stays ON state and S2 is turned ON in this mode. The input inductor L1 is charged again and the capacitors C1 and C2 are connected in series supplying power to the ac load.
Mode 6: S2 stays ON state and S1 is turned OFF in this mode. Similar as mode 5, the capacitors C1 and C2 are connected in series supplying power to the ac load.
Mode 7: S1 is turned ON in this mode. The inductor L1 is charged by the input dc source and the inductor current is increasing linearly. Meanwhile, the load current flows through S4 and anti parallel diode of S6.
Mode 8: S1 is turned OFF in this mode. Diodes D0 , D1 , and D2 are all conducting. The inductor L1 is discharging and the input source is charging the diode–capacitor network. In this mode, the ac load current still flows through S4 and anti parallel diode of S6.
Mode 9: S1 is maintained OFF and S5 is ON in this mode. Diodes D0 , D1 , and D2 are maintained ON. The input dc source charges the diode–capacitor cell and simultaneously provides the power to the load.
Mode 10: S1 is turned ON again while D0 is turned OFF in this mode. L1 is charged by the input source and capacitors C1 and C2 are working in parallel to feed the load.
Mode 11: S1 stays ON state and S2 is turned ON in this mode. The input inductor L1 is charged again and the capacitors C1 and C2 are connected in series supplying power to the ac load.
Mode 12: S2 stays ON state and S1 is turned OFF in this mode. Similar as mode 11, the capacitors C1 and C2 are connected in series supplying power to the ac load.

III PERFORMANCE ANALYSIS

The output voltage expression of the proposed converter and the comparison with other five-level inverters is performed in this section.

A. Output Voltage Derivation

In Stage I, since the sinusoidal modulating waveform does not intersect with the upper carrier waveform, S2 is maintained OFF and S3 is switching, as shown in Table I. Fig. 4 shows the possible switching states in Stage I. Depending on the duty cycle of S3 (ds3), two conditions could exist in the switching process in Stage I, i.e., dS3 < DS1 and dS3 > DS1 (shown in Zone A and Zone B, respectively, in Fig. 4). Ds1 is the duty cycle of switch S1 . In Stage II, S3 is maintained ON and S2 is switching since the modulating waveform intersects with the upper carrier waveform.
It is worth noting that the maximum duty cycle of S2 is set to be less than the duty cycle of S1 , i.e., S1 is definitely ON when S2 is ON, as shown in Fig. 5. Under this condition, modes 6 and 12 do not appear. Thus, the following inequality is satisfied:

$$A_m - 1 < D_{s1} \qquad (2)$$

where Am is the amplitude of the reference wave.

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The total current ripple of inductors L1 and Lo during one switching cycle of S1 ([t0, t4], [t5, t9] – Stage I, [t10, t14] – Stage II) can be derived as follows:

Equation3

where vR is the output voltage of the resistive load RL and Ts is the switching cycle of S1 .

By applying the principle of voltage–second balance on the inductor L1 , i.e., the inductor current ripple during one switching cycle is zero ($\Delta iL1[t0,t4] = \Delta iL1[t10,t14] = 0$), the mean capacitor voltage UC can be derived as

Equation4

Considering the current ripple of the output inductor Lo in (3), 1 + dS2 and dS3 are determined by the intersection of the reference waveform $A_m.sin\omega t$ with the upper and lower carrier, respectively. Hence, using (4), the output voltage of the resistor RL can be expressed as follows:

Equation5

The voltage gain (ratio between amplitude of load resistor voltage V_{Rm} and input voltage V_{in}) can be defined as follows:

Equation6

It can be seen that the voltage gain is dependent on amplitude of reference wave Am and duty cycle of S1. Once (2) is not satisfied, the output voltage is also dependent on the working time of modes 6 and 12 in one switching cycle.

IV SIMULATION RESULTS

MATLAB Simulation Circuit of the proposed single-phase step-up five-level inverter.

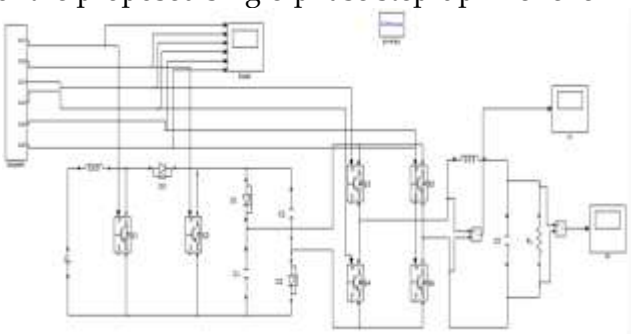

Fig. Simulation Circuit of the proposed single-phase step-up five-level inverter

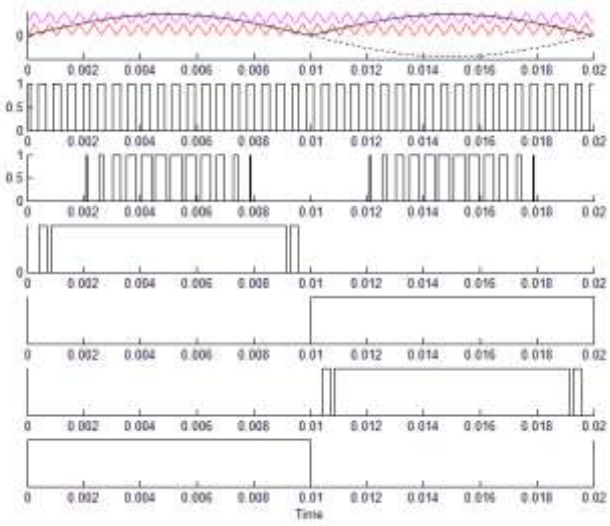

Fig. 2. Modulation method of the proposed step-up five-level inverter.

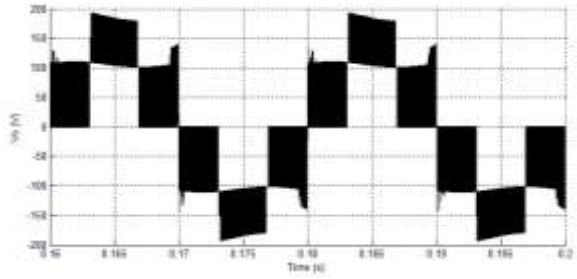

Fig. Simulation output voltage Vo result of the proposed inverter

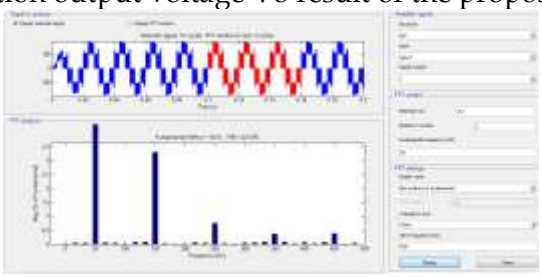

Fig. THD for output voltage Vo result of the proposed inverter

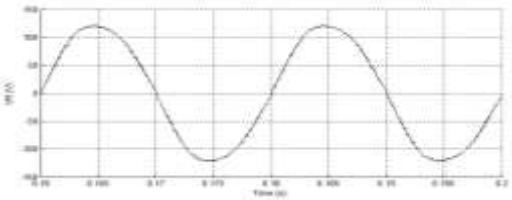

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Fig. Simulation load resistor voltage VR result of the proposed inverter

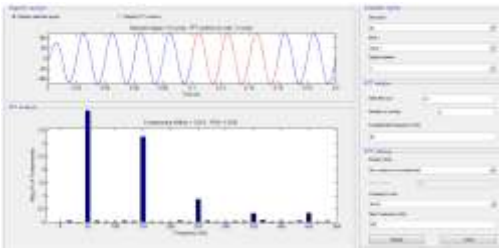

Fig. THD for load resistor voltage VR result of the proposed inverter

V CONCLUSION

This paper proposes an enhanced single-phase step-up five level inverter. Operating principle and output voltage derivation have been performed. Compared to conventional five-level topologies, the proposed inverter reduces the number of power switches, diodes, size and cost of the system. Simple structure, easy control, and high step-up voltage ratio are the main features of the proposed topology. In addition, only four switches are operated at high frequency and the overall switching losses are reduced. Finally, experimental results validate the effectiveness and performance of the proposed topolo
gy.

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