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NINE-LEVEL INVERTER FOR RENEWABLE POWER GENERATION SYSTEM

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Abstract

A nine-level inverter is developed and applied for injecting the real power of the renewable power into the grid to reduce the switching power loss, harmonic distortion, and electromagnetic interference caused by the switching operation of power electronic devices. A Four dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter configure the nine- level inverter. The input of the dual-buck converter is four dc capacitor voltage sources. The dual-buck converter converts four dc capacitor voltage sources to a dc output voltage with five levels and balances these four dc capacitor voltages.

I. INTRODUCTION

The conventional single-phase inverter topologies for grid connection include half- bridge and full bridge [1]–[4]. The half- bridge inverter is configured by one capacitor arm and one power electronic arm. The dc bus voltage of the half-bridge inverter must be higher than double of the peak voltage of the output ac voltage. The output ac voltage of the half-bridge inverter is two levels. The voltage jump of each switching is the dc bus voltage of the inverter. The full-bridge inverter is configured by two power electronic arms. The popular modulation strategies for the full-bridge inverter are bipolar modulation and unipolar modulation [3], [5]–[7]. The dc bus voltage of the full-bridge inverter must be higher than the peak voltage of the output ac voltage. The output ac voltage of the full- bridge inverter is two levels if the bipolar modulation is used and three levels if the unipolar modulation is used. The voltage jump of each switching is double the dc bus voltage of the inverter if the bipolar modulation is used, and it is the dc bus voltage of the inverter if the unipolar modulation is used. All power electronic switches operate in high switching frequency in both half-bridge and full bridge inverters. The switching operation will result in switching loss. The loss of power electronic switch includes the switching loss and the conduction loss. The conduction loss depends on the handling power of power electronic switch. The switching loss is proportional to the switching frequency, voltage jump of each switching, and the current of the power electronic switches. The power efficiency can be advanced if the switching loss of the dc–ac inverter is reduced.

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The output voltage of the dual-buck converter supplies to the full-bridge inverter. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility voltage to convert the output voltage of the dual-buck converter to a nine-level ac voltage. The output current of the five-level inverter is controlled to generate a sinusoidal current in phase with the utility voltage to inject into the grid. A hardware prototype is developed to verify the performance of the developed renewable power generationsystem

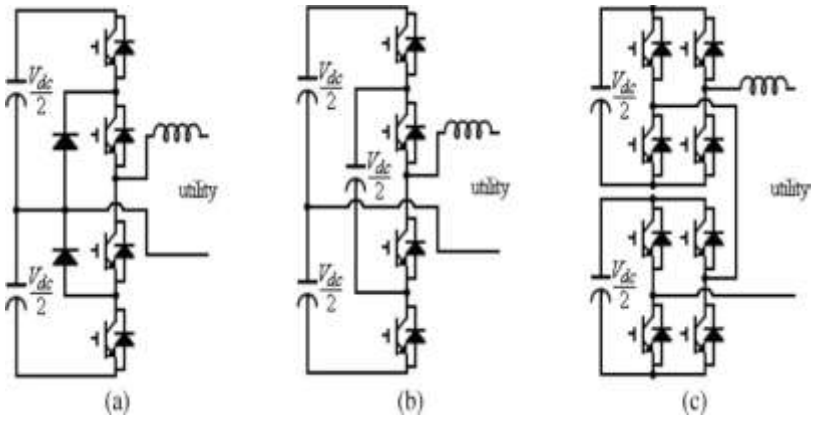

Fig. 1. Circuit configuration of conventional single-phase multilevel inverter.
(a) Diode clamped. (b) Flying capacitor. (c) Cascade H-bridge.

Multilevel inverter can effectively reduce the voltage jump of each switching operation to reduce the switching loss and increase power efficiency. The number of power electronic switches used in the multilevel inverter is larger than that used in the conventional half-bridge and full-bridge inverters. Moreover, its control circuit is more complicated. Thus, both the performance and complexity should be considered in designing the multilevel inverter [8], [9]. However, interest in the multilevel inverter has been aroused due to its advantages of better power efficiency, lower switching harmonics, and a smaller filter inductor compared with the conventional half-bridge and full-bridge inverters. The conventional single-phase multilevel inverter topologies include the diode-clamped.

The flying capacitor, and the cascade H-bridge types [10]–[15], as shown in Fig. 1. Fig. 1(a) shows the basic configuration of a diode-clamped multilevel inverter. As can be seen, it is configured by two dc capacitors, two diodes, and four power electronic switches. Two diodes are used to conduct the current loop, and four power electronic switches are used to control the voltage levels. The output voltage of the basic diode-clamped multilevel inverter has three levels. The voltage difference of each level is Vdc/2 (the voltage on a capacitor). Since the voltages of two dc capacitors are used to form the voltage level of the multilevel inverter, the voltages of these two dc capacitors must be controlled to be equal. The control for balancing these two dc capacitors is very important in controlling the diode-clamped multilevel inverter, and it is very hard under the light load [16]–[19]. If the nine-level output voltage is expected, extra four diodes and four power electronic switches are required [11], [20]. Fig. 1(b) shows the circuit configuration of a basic flying capacitor multilevel inverter. As can be seen, it is configured by three dc capacitors and four power electronic switches. The voltage on each dc capacitor is controlled to be Vdc/2, and the output voltage of the basic flying capacitor multilevel inverter has three levels. The voltage difference of each level is also Vdc/2 (the voltage on a dc capacitor). These three dc capacitors must be controlled for maintaining their voltages to be Vdc/2 in the charge and discharge processes. Therefore, its control circuit is more complicated. If nine-level output voltage is required, an extra dc capacitor and six power electronic switches are required [11], [13], [14]. Fig.2 shows the circuit configuration of the basic cascade H-bridge multilevel inverter [8]–[11], [15], [21]. As can be seen, it is configured by two full-bridge inverters connected in cascade. The dc bus voltage of each full-bridge inverter is Vdc/2, and the output voltage of each full-bridge inverter can be controlled to be Vdc/2, 0, and $-V$dc/2. Thus, the voltage levels of the output voltage of the cascade full-bridge multilevel inverter are Vdc, Vdc/2, 0, $-V$dc/2, and $-V$dc. This topology has advantages of fewer components being required compared with other multilevel inverters under the output voltage with the same levels, and its hardware circuit can be modularized because the configuration of each full bridge is the same. However, this topology has the disadvantages that two independent dc voltage sources are required.

In this project, a nine-level inverter is developed and applied for injecting the real power of the renewable power into the grid. This nine-level inverter is configured by four dc capacitors, a dual-buck converter, a full-bridge inverter, and a filter [22]. The nine-level inverter generates an output voltage with nine levels and applies in the output stage of the renewable power generation system to generate a sinusoidal current in phase with the utility voltage to inject into the grid. The power electronic switches of the dual-buck converter are switched in high frequency to generate a three-level voltage and balance the two input dc voltages. The power electronic switches of the full-bridge inverter are switched in low frequency synchronous with the utility to convert the output voltage of the dual- buck converter to a nine-level ac voltage. Therefore, the switching power loss, harmonic distortion, and electromagnetic interference (EMI) caused by the switching operation of power electronic devices can be reduced, and the control circuit is simplified. Besides, the capacity of output filter can be reduced. A hardware prototype is developed to verify the performance of the developed renewable power generation system.

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II. CIRCUIT CONFIGURATION

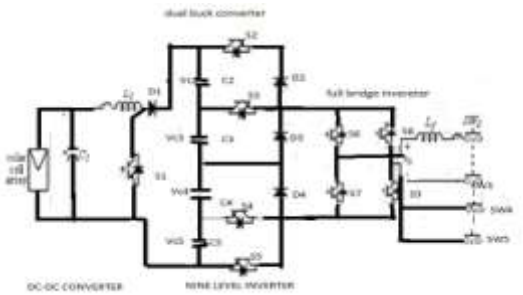

Fig. 2 shows the circuit configuration of the nine-level inverter

It is configured by a solar cell array, a dc– dc converter, a nine-level inverter, four Switches *SW*1, *SW2, SW3, SW4* are placed between those switches and they are used to disconnect the photovoltaic power generation system from the utility when islanding operation occurs. The output of the solar cell array is connected to the input port of the dc–dc converter. The output port of the dc–dc converter is connected to the nine- level inverter. The dc–dc converter is a boost converter, and it performs the functions of maximum power point tracking (MPPT) and boosting the output voltage of the solar cell array. This nine-level inverter is configured by four dc capacitors, a dualbuck converter, a full-bridge inverter, and a filter. The dual-buck converter is configured by two buck converters. The four dc capacitors perform as energy buffers between the dc–dc converter and the nine- level inverter. The output of the dual-buck converter is connected to the full-bridge inverter to convert the dc voltage to ac voltage. An inductor is placed at the output of the fullbridge inverter to form as a filter inductor for filtering out the high-frequency switching harmonic generated by the dual- buck converter.

III. VOLTAGE BALANCING OF NINE- LEVEL INVERTER

Balancing the voltages of dc capacitors is very important in controlling the multilevel inverter. The voltage balance of dc capacitor voltages *VC*2 and *VC*3 can be controlled by the power electronic switches *S*2, *S3, S4, and S5* easily. When the absolute of the utility voltage is smaller than *V*dc/2, one power electronic switch either *S*2 or *S*3 is switched in high frequency and the other is still in the OFF state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages *VC*2 and *VC*3. If dc capacitor voltage *VC*2 is higher than dc capacitor voltage *VC*3, power electronic switch *S*2 is switched in high frequency. In this situation, the voltage source *VC*2 and *C*2 will be discharged. Thus, the dc capacitor voltages *VC*2 decreases and *VC*3 does not change. On the contrary, power electronic switch *S*3 is switched in high frequency when voltage *VC*3 is higher than voltage *VC*2. In this situation, the voltage source .Thus, the dc capacitor voltages *VC*3 decreases and *VC*2 does not change. In this way, the voltage balance of *C*2 and *C*3 can be achieved. When the absolute of the utility voltage is higher

than *V*dc/2, one power electronic switch either *S*2 or *S*3 is switched in high frequency and the other is still in the ON state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages *VC*2 and *VC*3. If dc capacitor voltage *VC*2 is higher than dc capacitor voltage *VC*3, the power electronic switch *S*3 is switched in high frequency. The voltage source *VCx* in Fig.2 is dc capacitor voltage *VC*2. When the power electronic switch *S*3 is turned ON, both *C*2 and *C*3 are discharged however, only *C*2 supplies the power when the power electronic switch *S*3 is turned OFF. Thus, *C*2 will discharge more power than that of *C*3. On the contrary, the power electronic switch *S*2 is switched in high frequency when dc capacitor voltage *VC*3 is higher than dc capacitor voltage *VC*2 The voltage source *VCx* in Fig.2 is dc capacitor voltage *VC*3. When the power electronic switch *S*2 is turned ON, both *C*2 and *C*3 are discharged. However, only *C*3 supplies the power when the power electronic switch *S*2 is turned OFF. Thus, *C*3 will discharge more power than that of *C*2. In this way, the voltage balance of *C*2 and *C*3 can be achieved. As mentioned earlier, the operation of power electronic switches *S*2 and *S*3 can be summarized as Table I. The voltages of capacitors *C*2 and *C*3 can be easily balanced compared with the conventional multilevel inverter.

If dc capacitor voltage *VC*4 is higher than dc capacitor voltage *VC*3, power electronic switch *S*4 is switched in high frequency. In this situation, the voltage source *VC*4 and *C*4 will be discharged. Thus, the dc capacitor voltages *VC*4 decreases and *VC*3 does not change. On the contrary, power electronic switch *S*3 is switched in high frequency when voltage *VC*3 is higher than voltage *VC*4. In this situation, the voltage source .Thus, the dc capacitor voltages *VC*3 decreases and *VC*4 does not change. In this way, the voltage balance of *C*4 and *C*3 can be achieved. When the absolute of the utility voltage is higher than *V*dc/2, one power electronic switch either *S*4 or *S*3 is switched in high frequency and the other is still in the ON state. Which power electronic switch is switched in high frequency depends on the dc capacitor voltages *VC*4 and *VC*5. If dc capacitor voltage *VC*24 is higher than dc apacitor voltage *VC*5, the power electronic switch *S*3 is switched in high frequency

IV. CONTROL BLOCK DIAGRAM

The developed photovoltaic power generation system consists of a dc–dc power converter and the nine-level inverter. The nine-level inverter performs the functions of converting the dc power into high-quality ac power and injecting it into the utility, balancing four dc capacitor voltages *VC*2,*VC*3,*VC4*,*VC5* , and detecting the islanding operation. The dc–dc converter boosts the output voltage of the solar cell array and performs the MPPT to extract The maximum output power of the solar cell array. The controllers of both the dc–dc converter and the nine-level inverter are explained as follows.

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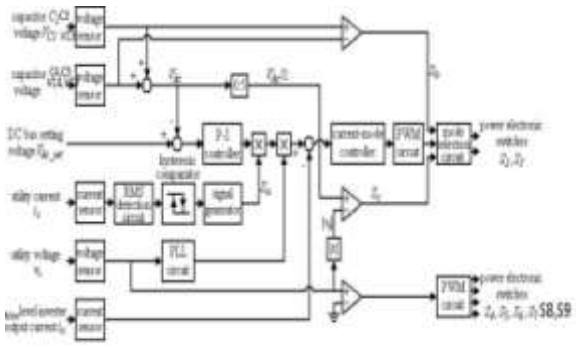

Fig.3 block diagram

A. Nine-Level Inverter

Fig. 3 shows the control block diagram of nine-level inverter. In the operation of the nine-level inverter, the dc bus voltage must be regulated to be larger than the peak voltage of the utility, and the dc capacitor voltages of *C*2,*C*3,C4,C5 must be controlled to be equal. Besides, the nine-level inverter must generate a sinusoidal current in phase with the utility voltage to be injected into the utility. As seen in Fig. 3, the voltages of dc capacitors *C*2, *C3, C4, C5* are detected and then added to obtain a dc bus voltage *V*dc. The added result is subtracted from a dc bus setting voltage *Vdcset* The dc bus setting voltage *Vdcset* is larger than the peak voltage of the utility. The subtracted result is sent to a P-I controller. An islanding detection is also incorporated into the control of the nine-level inverter. The concept of this islanding detection was proposed by authors [23]. However, it will not be addressed in this project.

As seen in Fig. 3, the utility current is detected and sent to an RMS detection circuit. The output of the RMS detection circuit is sent to a hysteresis comparator that contains a low threshold value and a high threshold value. If the RMS value of the utility current is smaller than the low threshold value, the output of the hysteresis comparator is high, meaning the condition of islanding operation or power balance occurs. On the contrary, the output of the hysteresis comparator is low when the RMS value of the utility current is larger than the high threshold value, meaning the utility is normal. The output of the hysteresis comparator is sent to a signal generator. The output signal of the signal generator is an islanding control signals *Sa* The islanding control signal is a dc signal with unity amplitude if the output of the hysteresis comparator is low. On the contrary, the islanding control signal is a square wave with a frequency of 20 Hz (disturbance signal for islanding detection) when the output of the hysteresis comparator is high. The outputs of the PI controller and signal generator are sent to a multiplier, and the product of the multiplier is the amplitude of the reference signal. The utility voltage is detected and then sent to a phase-lock loop (PLL) circuit to generate an unity-amplitude sinusoidal signal whose phase is in phase with the utility voltage. The outputs of the multiplier and the PLL circuit are sent to the other multiplier. The product of this

multiplier is the reference signal of the output current for the nine-level inverter.

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The output current of the nine-level inverter is detected by a current sensor. The reference signal and detected signal for the output current of the nine-level inverter are sent to a subtractor. The subtracted result is sent to a current-mode controller. The output of the current-mode controller is sent to a PWM circuit to generate a PWM signal. The detected dc capacitor voltages *VC2, VC3, VC4, VC5* are also sent to a comparator to obtain signal *Sb* . When dc capacitor voltage *VC*2 is higher than dc capacitor voltage *VC*3, *Sb* is a high value. On the contrary, *Sb* is a low value when dc capacitor voltage *VC*2 is smaller than dc capacitor voltage *VC*3. DC voltage *V*dc is also sent to an amplifier with a gain of 0.5 to obtain voltage signal *V*dc/2. The detected utility voltage is sent to an absolute circuit to obtain voltage signal $|vs|$. Voltage signals *V*dc/2 and $|vs|$ are compared to obtain signal *Sc* . When *V*dc/2 > $|vs|$, *Sc* is a high value. On the contrary, *Sc* is a low value when *V*dc/2 < $|vs|$. The output signal of the PWM circuit and signals *Sb* and *Sc* are sent to the mode selection circuit. The output of the mode selection circuit will generate the control signals of power electronic switches *S*2,S3,S4 and S5. The detected utility voltage is also sent to a comparator to obtain complementary square signals that are synchronous with the detected utility voltage. The complementary square signals are the control signals of the power electronic switches of the full-bridge inverter. As mentioned earlier, only four power electronic switches in the nine-level inverter should be switched in high frequency, and only one of them is switched in high frequency at any time, and the voltage level of every switching is *V*dc/2. Therefore, the nine-level inverter can reduce the switching loss effectively.

B. **DC–DC Converter**

Fig. 4 shows the control block of the dc–dc converter. The input of the dc–dc converter is the output of the solar cell array.

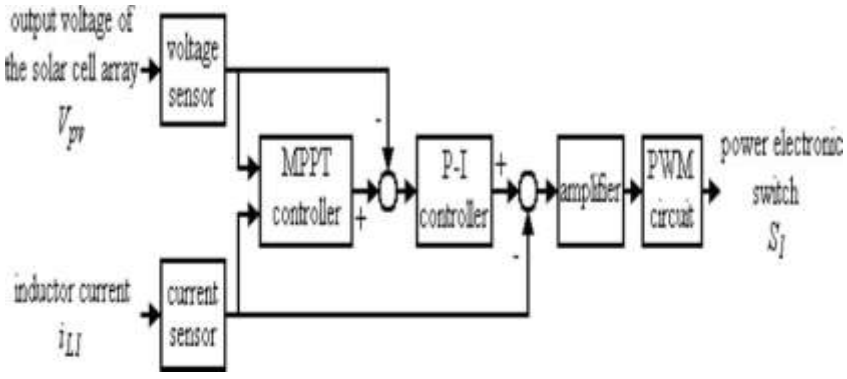

Fig. 4. Control block of the dc–dc converter

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A ripple voltage with a frequency double that of the utility will appear in the dc bus voltage *V*dc, while the nine-level inverter injects real power into the utility. The function of MPPT will be degraded, while the output voltage of solar cell array contains a Ripple voltage. Therefore, the ripple voltage superimposed on the dc bus voltage *V*dc must be blocked by the dc–dc converter for improving the function of MPPT. Accordingly, the dual control loops, an outer voltage control loop, and an inner current control loop are applied to control the dc–dc converter. Since the output voltage of the dc–dc converter is the dc bus voltage that is controlled to be a constant voltage by the nine-level inverter, the outer voltage control loop is used to regulate the output voltage of the solar cell array. The inner current control loop is applied to control the inductor current to approach a constant current to block the ripple voltage of dc bus voltage *V*dc. The perturbation and observation method is adopted to obtain the function of MPPT [24], and it is incorporated into the controller of the dc– dc converter. The output of the MPPT controller is the desired output voltage of the solar cell array, and it is the reference voltage of the outer voltage control loop. The output voltage of the solar cell array is perturbed first, and then the output power variation of the solar cell array is observed to determine the next perturbation for the output voltage of the solar cell array. The output power of the solar cell array is calculated from the product of the output voltage of the solar cell array and the inductor current. Therefore, the output voltage of the solar cell array and the inductor current are detected and sent to a MPPT controller to determine the desired output voltage of the solar cell array. The detected output voltage and desired output voltage of the solar cell array are sent to a subtractor, and the subtracted result is sent to a P-I controller. The output of the P-I controller is the reference signal of the inner current control loop. The reference signal and the detected inductor current are sent to a subtractor, and the subtracted result is sent to an amplifier to complete the inner current control loop. The output of the amplifier is sent to the PWMcircuit. The output signal of the PWM circuit is the driving signal for the power electronic switch of the dc–dc converter. For protecting the renewable power generation system from the voltage rise, the MPPT function will be disabled and the power electronic switch *S*1 will be turned OFF when the inverter stage is interrupted after detecting the islanding operation. Therefore, the output voltage of solar cell array is limited to the open-circuit voltage of solar cell array, and the dc bus voltage *V*dc is also limited.

MAJOR PARAMETERS USED IN THE PROJECT

Solar module	
Rate of maximum power	75W
Open voltage	21.7V
Short current	5.0A
DC-DC converter	
Capacitor (C_1)	470μF
Inductor (L_1)	2mH
Switch frequency	20kHz
Five-level inverter	
DC bus capacitor (C_2 and C_3)	2,200μF
Filter inductor (L_f)	1.4mH
DC bus setting voltage	170V
Switch frequency (PWM)	20kHz
Utility voltage	110V
Utility frequency	60Hz

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V. EXPERIMENTAL RESULTS

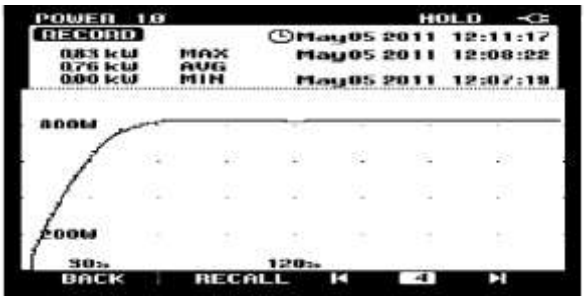

Fig. 5. Experimental results of MPPT performance for the developed photovoltaic power generation system.

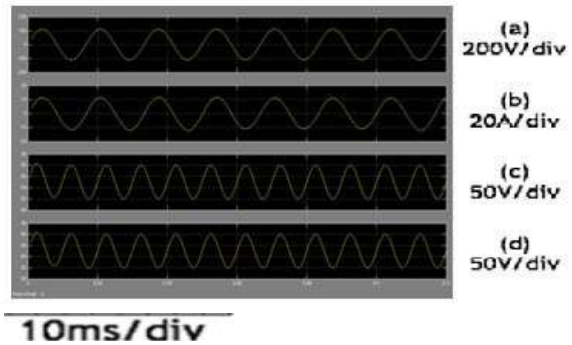

Fig. 6 Experimental results of nine level inverter (a) utility voltage (b)o/p current of nine level inverter (c)dc capacitor voltage vc2 (d). d.c capacitor voltage vc3

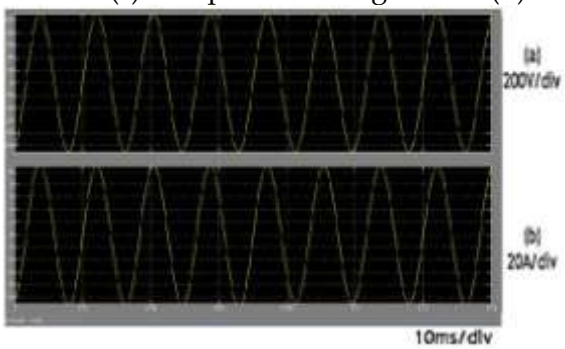

Fig.7. Experimental results for the developed photovoltaic power generation system under the distorted utility voltage. (a) Utility Voltage. (b) Output current of the nine-level inverter.

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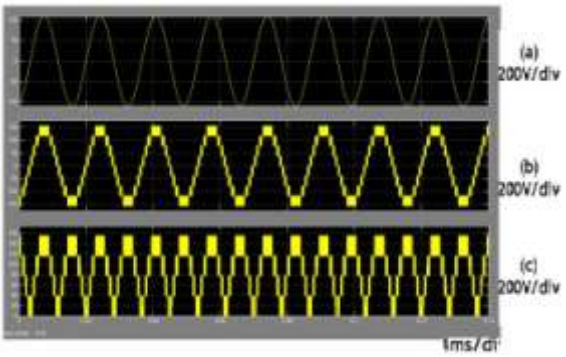
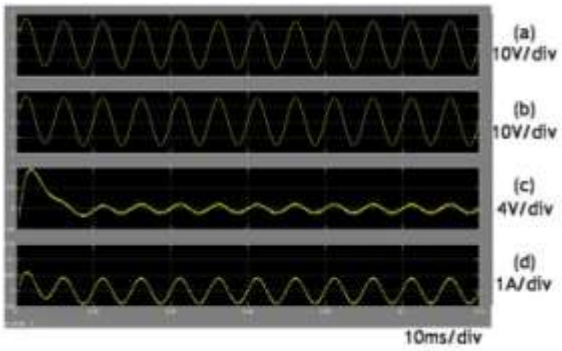


Fig. 8. Experimental results of the nine-level inverter. (a) Utility voltage. (b) Output voltage of the full-bridge inverter.



(c) Output voltage of the dualbuck converter

Fig. 9. Experimental results for the dc–dc converter of the developed photovoltaic power generation system. (a) Voltage ripple of dc capacitors *C*2,C4 . (b) Voltage ripple of dc capacitors *C*3,C5 . (c) Output voltage ripple of solar cell array. (d) Inductor current ripple of dc–dc converter

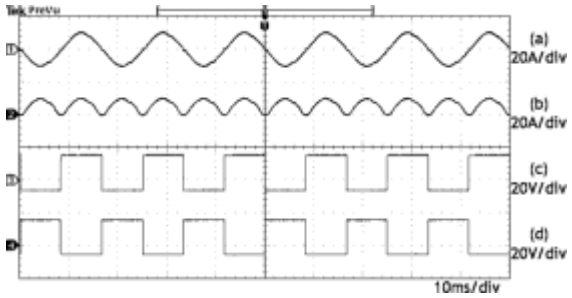


Fig. 10. Experimental results for full-bridge inverter of the nine-level inverter. (a) Output current of the full-bridge inverter *io* . (b) Input current of the fullbridge inverter *i*dc . (c) Driver signal of *S*4 . (d) Driver signal ofS5 .

Fig. 5, the output power of the solar cell array in the developed photovoltaic power generation system is about 830 W. Therefore, the developed photovoltaic power generation system can track the maximum power point of the solar cell array effectively. Fig. 6 shows the experimental results for the nine-level inverter used in the developed photovoltaic power generation.Fig. 6 shows the experimental results for the nine-level inverter used in the developed photovoltaic power generation system under the steady state. The output power of the solar cell array is about 830 W.

As seen in the output current of the nine- level inverter is sinusoidal and in phase with the utility voltage. The total harmonic distortion (THD%) of the utility voltage and the output current of the nine-level inverter are 4.1% and 3.3%, respectively.

Fig. 9 shows the experimental results for the dc–dc converter of the developed photovoltaic power generation system. Fig. 9(a) and (b) show the peak-to-peak value of the voltage ripple at dc capacitors *C*2 and *C*3 is about 7 V. Fig. 9(c), the peak-to-peak value of the voltage ripple at the solar cell array is only bout 1.6 V. Fig. 9(d) shows the ripple of the inductor current is very small due to the use of the current mode control. In this way, the output voltage of the solar cell array can be more stable. This verifies that the developed control method for the dc–dc converter of the developed photovoltaic power generation system can effectively block the voltage ripple of nine-level inverter delivering to the output voltage of the solar cell array. Fig. 10 shows the experimental results for the full-bridge inverter of the nine-level inverter. As can be seen, the input current *i*dc of the full-bridge inverter shown in Fig. 10(b) is the absolute of the output current of the full-bridge inverter shown in Fig. 10(a). As seen in Fig. 10(c) and (d), the switch frequency of the power electronic switches *S*4 and *S*5 is 60 Hz. This verifies the power electronic switches of the full-bridge inverter are switched in low frequency, and the full- bridge inverter can convert the dc power into ac power by commutating.

Fig. 8 shows the experimental voltage of the nine-level inverter. As seen in Fig. 8(c), the dual-buck converter outputs a dc voltage with three levels *V*dc, *V*dc/2, and 0output voltage of the dual-buck converter is further converted to an ac voltage with nine voltage levels Vdc/4,3Vdc/4.-Vdc/4,-3Vdc/4,*V*dc, *V*dc/2, 0, −*V*dc/2, and −*V*dc by the full- bridge inverter. The voltage variation of each level is *V*dc/2. This verified that the nine-level inverter can generate a nine-level output ac voltage according to the utility voltage and only the power electronic switches of the dual-buck converter is switched in high frequency.

VI. CONCLUSION

A photovoltaic power generation system with a nine-level inverter is developed in this project. The nine-level inverter can perform the functions of regulating the dc bus voltage, converting solar power to ac power with sinusoidal current and in phase with the utility voltage, balancing the four dc capacitor voltages, and detecting islanding operation. The experimental results

verify the developed photovoltaic power generation system, and the nine-level inverter achieves the expected performance.

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