

## **A FULLY INTEGRATED THREE-LEVEL ISOLATED SINGLE -STAGE PFC CONVERTER**

**#1V.BHARGAVI, PG STUDENT**

**#2Mr.E.RAMAKRISHNA, Associate Professor**

**St. John's College of Engineering & Technology, Yerrakota, Yemmiganur.**

**#3Dr.A.Mallikarjuna Prasad, Associate professor, Dept of EEE,  
Vardhaman College of Engineering, Hyderabad, Telangana, India**

---

### *Abstract*

*A fully integrated three-level isolated single-stage PFC ac/dc converter is proposed for low power applications. The proposed converter exhibits high PF with less number of switches/diodes, operated at constant duty ratio. An inductor and a diode bridge are added to the conventional three-level isolated dc/dc converter, with a modified switching scheme and fuzzy based controller. The input current ripple frequency is twice of the switching frequency contributing to using smaller PFC inductor. Moreover, output current and voltage ripples are very less. A high PF is achieved by this topology. Fuzzy controller is used which has the advantage of fast response.*

### **I.INTRODUCTION**

In ac/dc power converters are required to operate with high power factor (PF) and low total harmonic distortion (THD) for improved grid quality and full capacity utilization of the transmission lines. Passive PF correction (PFC) circuits consist of inductive and capacitive filters followed by a diode bridge provide the simplest way of achieving high PF with high efficiency; however, they require low line frequency filters which are bulky and heavy. In order to operate at high frequency and reduce the size of the circuit, high frequency two-stage active PFC converters have been proposed. In this architecture, a front-end ac/dc PFC converter is operated with a switching frequency in the order of tenths to several hundred kHz for converters with Si semiconductor devices, and from several hundreds of kHz to tenths of MHz with wide-band gap devices, to shape the input current close to sinusoidal waveform in phase with the grid voltage. The second stage dc/dc converter provides the galvanic isolation and output voltage regulation. The controllers of the two stages are completely independent. The flexibility in control allows optimizing power stages, fast output voltage regulation and operating with high PF and low THD. However, this method comes with the expense of more components and larger size. Moreover, the constant switching losses such as parasitic capacitance losses associated with power switches reduce the efficiency of the converter at light load condition. A cost-effective approach to reduce the number of switches is to use single-stage ac/dc converters. In single-stage PFC converters, the front-end PFC stage and dc/dc stages are integrated and their operations are performed in a single-stage, basically, by sharing some of the switches and control scheme. An energy storage unit, capacitor or inductor, is located in between two stages, acting as a power buffer and providing sufficient hold up time. Numerous PFC ac/dc single-stage topologies have been proposed in literature, particularly, operating in discontinuous conduction mode (DCM) for simple yet effective PF control.

Majority of the proposed single-stage converters are proposed for low-power applications, where a fly back or forward converter derived topologies are used to achieve input current shaping and output voltage regulation. These converters offer cost-effective solution for low-power applications; however, they suffer from excessive voltage/current stresses on the switches, and are suitable for power levels lower than 200 W. For medium to high power applications, the research efforts have focused on ac/dc single-stage full-bridge (SSFB) converters. Current-fed SSFB converters deploy a current shaping inductor connected to the input of the diode-bridge achieving high PF; however, due to the lack of dc bus capacitor on the primary side of the transformer, the dc bus voltage is subjected to excessive overshoots and ringing. Furthermore, the output voltage contains high amplitude second-order harmonic oscillating with twice the line frequency, which restricts their operation. Voltage-fed SSFB converters do not exhibit the drawbacks of current-fed SSFB converters, where a large capacitor is located on the primary side dc bus. However, the dc bus voltage remains unregulated and it can be excessive at light load condition, as both input current shaping and output regulation are achieved with a single controller.

In the literature, resonant converters adopting variable switching frequency have been proposed. In these converters, it is difficult to tune the resonant tank components over a wide load range, and optimize EMI filter. In majority of these aforementioned converters, the output current ripple becomes very large and the converter operation may transit to DCM mode. In two-level SSFB converters, the switches are exposed to high voltage stresses; thus, dc-link voltage is typically set close to 400 V. In multilevel configurations, the voltage stresses across the switches are significantly reduced. Quite recently, single stage three-level (SSTL) converters have been studied, which allow a flexible dc-link voltage in the range of 400 to 800 V. A resonant SSTL converter is proposed to alleviate the drawbacks associated with SSFB converters, while reducing the voltage stress on the switches. In a recent publication, a three-level converter is integrated with the PFC boost stage by sharing the bottom switch. It is aimed to decouple the dc bus voltage and output voltage controllers, while the input current is adjusted with a constant duty cycle in DCM mode. The duty cycle of the bottom switch shapes the input current as well as is used to transfer energy from dc bus to output, simultaneously. The required duty cycle is the sum of the values achieved from individual PI controllers. The output voltage regulator sets the base duty cycle, while the PI controller of dc bus voltage regulator extends the duty cycle for the bottom switch.

This topology alleviates most of the problems associated with SSFB converters, operated at constant switching frequency with a flexible dc-link voltage. However, two auxiliary diodes are added to 1) prevent input current to flow through the midpoint of split dc bus capacitors, and 2) enable a freewheeling path for primary side current when the energy in the leakage inductance is transferred to the bottom capacitor. In addition, a third auxiliary diode is added to serve as a boost PFC diode. Although the converter proposed in has been proven to work, it can further be integrated for lower power applications by removing the auxiliary diodes and developing a phase shifted modulation scheme. This study proposes a new SSTL isolated ac-dc PFC converter for high dc-link voltage and low-power applications, achieved with complete integration of two stages, where all of the switches are shared between input current shaping and output voltage regulation stages, as shown in Fig. 1.

In comparison with the existing three-level single-stage topologies, the proposed converter offers

minimum number of components as of three-level dc/dc converter, and does not require any auxiliary circuit other than a diode bridge and an inductor. The proposed topology can serve as a low cost power electronic interface intended for applications requiring high-voltage dclink. Two independent control algorithms, embedded in a single microcontroller, are used to achieve PFC and output voltage regulation. This feature allows having lower output current ripple and less distorted input current even at light load condition. In addition, the middle two switches are turned ON under zero current in DCM operation, and the upper and bottom switches are turned on under zero voltage, which increases the efficiency of the converter in comparison to hard-switched ac/dc single-stage converter. Furthermore, higher PF can be achieved at high line voltage due to the flexible dc-link voltage structure.

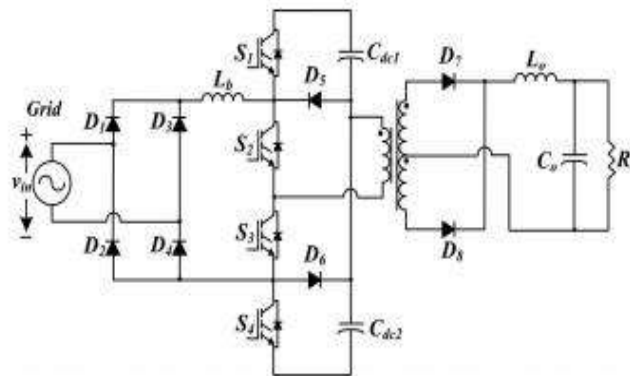


Fig 1: Proposed three-level single-stage fully integrated PFC ac-dc converter

## II. BOOST CONVERTER

A boost converter (step-up converter) is a power converter with an output DC voltage greater than its input DC voltage. It is a class of switching-mode power supply (SMPS) containing at least two semiconductor switches (a diode and a transistor) and at least one energy storage element. Filters made of capacitors (sometimes in combination with inductors) are normally added to the output of the converter to reduce output voltage ripple.

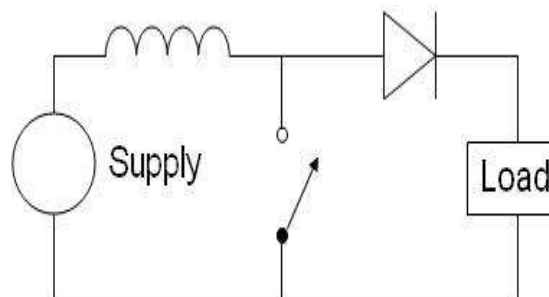


Fig 2: Schematic Diagram of Boost Converter

Power can also come from DC sources such as batteries, solar panels, rectifiers and DC generators.

A process that changes one DC voltage to a different DC voltage is called DC to DC conversion. A boost converter is a DC to DC converter with an output voltage greater than the source voltage. A boost converter is sometimes called a step-up converter since it "steps up" the source voltage. Since power ( $P = VI$  or  $P = UI$  in Europe) must be conserved, the output current is lower than the source current. A boost converter may also be referred to as a 'Joule thief'. This term is usually used only with very low power battery applications, and is aimed at the ability of a boost converter to 'steal' the remaining energy in a battery. This energy would otherwise be wasted since a normal load wouldn't be able to handle the battery's low voltage. This energy would otherwise remain untapped because in most low-frequency applications, currents will not flow through a load without a significant difference of potential between the two poles of the source (voltage.)

### **III. OPERATION OF THREE-LEVEL SINGLE-STAGE PFC CONVERTER**

The proposed converter is essentially an integrated version of a boost PFC circuit and three-level isolated dc-dc converter. Basically, a diode bridge and an inductor are added to the three level isolated dc-dc converter topology as shown in Fig. 3(a). Here, the inductor is charged when S2 and S3 are turned on simultaneously. Body diodes of S1 and S4 serve as the boost diode of the PFC boost converter. At the same time, S1 to S4 are switched to apply  $V_{dc}/2$ ,  $-V_{dc}/2$ , and zero voltage across the primary side of the transformer. Thus, all of the switches are shared between the two-stages, which makes it fully integrated single-stage converter without any additional auxiliary switches.

The switching scheme of the conventional three-level isolated dc/dc converter is given in Fig. 3(b). In this conventional scheme, the duty ratios of S2 and S3 are fixed close to 50% for simplicity in control and to ensure upper or lower three switches are not turned ON simultaneously as this would cause short-circuit through dc-link capacitors. Overlapping these two signals, as long as short-circuit condition is avoided, has no impact on the operation of the circuit. Similar to that in the conventional scheme, zero voltage is applied across the primary side of the transformer. This modified switching scheme is presented in Fig. 3(c).

When a boost inductor and a diode bridge is added to the nodes as in Fig. 3(a), the overlap of gate signals of S2 and S3 enables applying input voltage across the boost inductor. The switching scheme of the converter is given in Fig. 4. The switches S2 -S3 , and S1 -S4 have 180° phase shift with respect to each other. The duty ratios of S2-S3 should be greater than 0.5 such that two signals overlap. Here, the circuit is explained considering that input inductor current is discontinuous and the switching scheme is as follows; S1 is turned on right after S3 is turned OFF, and similarly, S4 is turned on when S2 is turned OFF. A dead-time should be inserted in between the turning ON instant of S1 and turning OFF instant of S3 , and likewise between switching of S2 and S4 to avoid short-circuit.

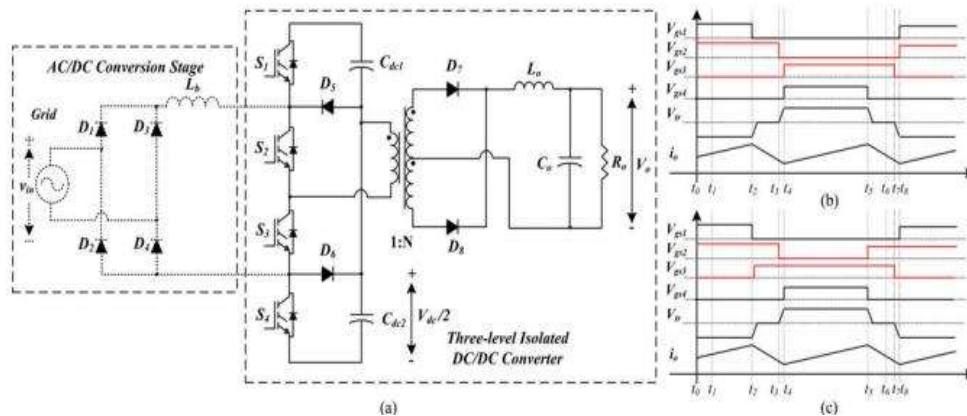


Fig 3. Derivation Of The Proposed Single-Stage PFC Converter; (A) Topology, (B) Switching Scheme Of The Conventional Three-Level Dc/Dc Converter, And (C) Modified Switching Scheme

### 3.1 operating Modes:

The operation modes of the circuits, which are given in Fig. 4, are explained in this section.

**Mode 1 [ $t_0 < t < t_1$ ]:** In this mode, both S1 and S2 are on. The upper capacitor, Cdc1, discharges to the load by applying  $-V_{dc}/2$  to the primary side of the transformer. The primary side current increases linearly under constant voltage. D8 conducts at the secondary side of the transformer. The voltage across the output inductor is  $V_{Lo} = V_{dc}/2N - V_o$ . In this mode, the boost inductor,  $L_b$ , does not interfere to the operation of the circuit.

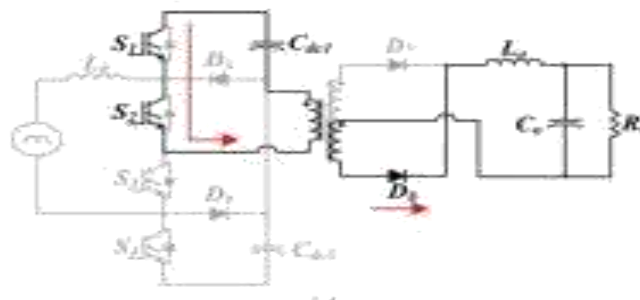
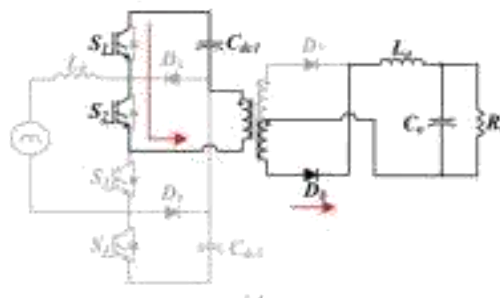


Fig 4 (a) Mode 1:  $t_0 < t < t_1$ .



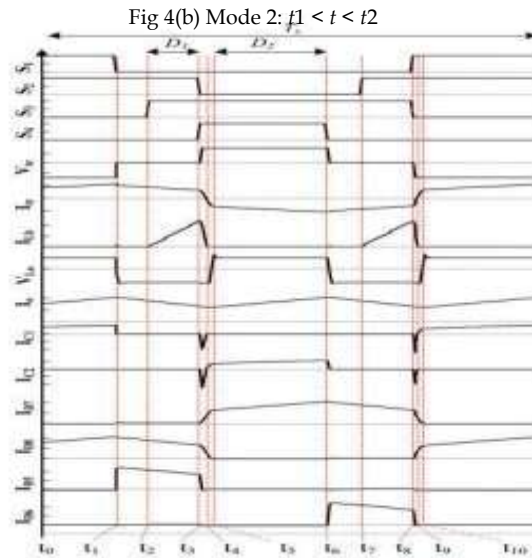


Fig 4. Switching Scheme Of The Proposed Integrated Three-Level Ac-Dc Converter

**Mode 2 [ $t_1 < t < t_2$ ]:** At  $t = t_1$ ,  $S_1$  is turned OFF and  $S_2$  is kept on. The current in the leakage inductance conducts  $D_5$  and the primary side current freewheels; hence, zero voltage is applied across the primary side of the transformer. The output inductor voltage is equal to  $-V_o$ . The output inductor current decreases linearly.

**Mode 3 [ $t_2 < t < t_3$ ]:** At  $t = t_2$ ,  $S_3$  is turned on, while  $S_2$  still remains on. The primary current continuous to freewheel and zero voltage is applied across the primary side; hence, the output inductor current continuous to decrease under output voltage. Meantime,  $V_{in}$  is applied across  $L_b$ , and input current increases linearly storing energy in the inductor.

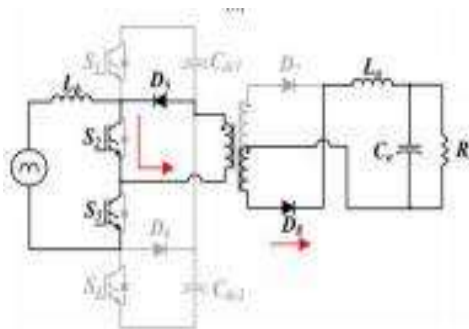


Fig 4 (c) Mode 3:  $t_2 < t < t_3$

**Mode 4 [ $t_3 < t < t_5$ ]:** In the beginning of this mode,  $S_2$  is turned OFF,  $S_4$  is turned ON, while  $S_3$  is kept on. Within this time interval, the following two operations are completed. The energy stored in the input inductor is transferred to the dc-link capacitors. The inductor current decreases linearly under  $V_{in} - V_{dc}$ . Meantime,  $V_{dc}/2$  is applied across the primary side of the transformer. The current in the leakage inductance is transferred to  $C_{dc2}$ .

This causes the output current to commute from D8 to D7 . At the end of this time interval, the energy in the input inductor is completely transferred to the dc-link capacitors and the commutation of the output diodes is completed. Depending on the dc bus voltage, and input current, one of these operations ends earlier than the other one. In this case, the energy stored in Lb is transferred to the dc-link at  $t = t_5$ . Then, the current commutation from D8 to D7 is completed at  $t = t_6$ .

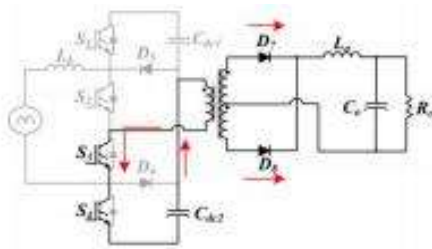


Fig 4 (c) Mode 3:  $t_3 < t < t_4$

**Mode 5 [ $t_5 < t < t_6$  ]:** Cdc2 discharges over to the load and  $V_{dc}/2$  is applied across the primary side of the transformer. The voltage across the output inductor is  $V_{Lo} = V_{dc}/2N - V_o$  . The input current remains at zero in DCM mode.

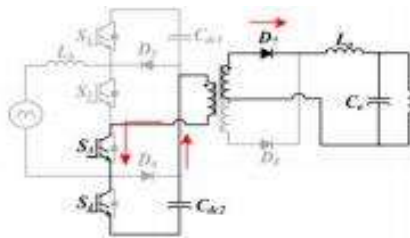


Fig 4 (d) Mode 5:  $t_5 < t < t_6$

**Mode 6 [ $t_6 < t < t_7$  ]:** At  $t = t_6$  , S4 is turned OFF, and only S3 is on. This allows leakage current to freewheel through D6, and zero voltage is applied to the primary side. The output current decreases linearly under  $-V_o$ .

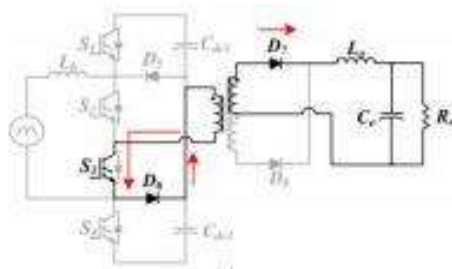


Fig 4 (e) Mode 6:  $t_6 < t < t_7$

**Mode 7 [ $t_7 < t < t_8$  ]:** At  $t = t_7$  , S2 is turned ON. The energy from the input is stored in the

inductor. This is similar to Mode 3, except that this time the primary side current is opposite to that in Mode 3 and freewheels through D6. Mode 8 [ $t_8 < t < t_{10}$ ]: At the beginning of this interval, S3 is turned OFF, S1 is turned ON, and S2 remains ON. This mode is similar to Mode 4, where the stored energy in the inductor is transferred to the dc bus capacitors, and  $-V_{dc}/2$  is applied to the primary windings. In the meantime, the output inductor current commutates from D7 to D8.

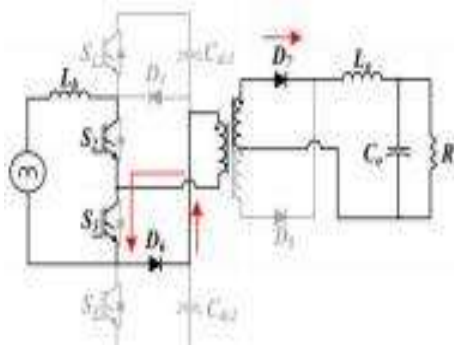


Fig 4 (f) Mode 7:  $t_7 < t < t_8$ .

**Mode 8 [ $t_8 < t < t_{10}$ ]:** At the beginning of this interval, S3 is turned OFF, S1 is turned ON, and S2 remains ON. This mode is similar to Mode 4, where the stored energy in the inductor is transferred to the dc bus capacitors, and  $-V_{dc}/2$  is applied to the primary windings. In the meantime, the output inductor current commutates from D7 to D8.

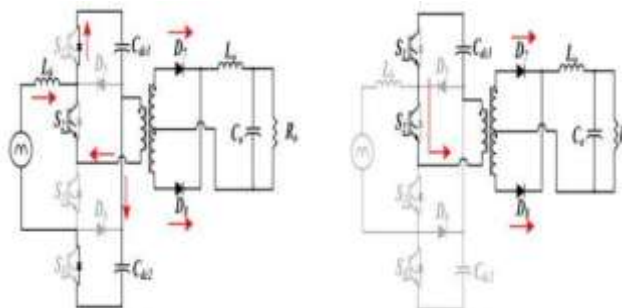


Fig 4 (g) Mode 8:  $t_7 < t < t_8$  and (j)  $t_8 < t < t_9$

## V.FUZZY LOGIC

In recent years, the number and variety of applications of fuzzy logic have increased significantly. The applications range from consumer products such as cameras, camcorders, washing machines, and microwave ovens to industrial process control, medical instrumentation, decision-support systems, and portfolio selection. To understand why use of fuzzy logic has grown, you must first understand what is meant by fuzzy logic.



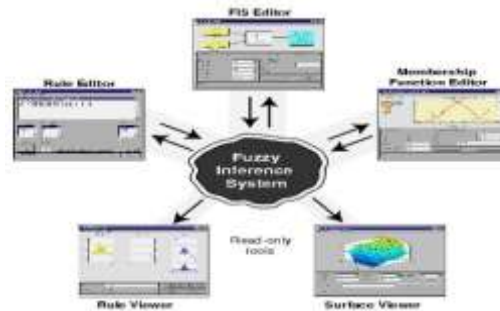


Fig 5. The Primary GUI Tools Of The Fuzzy Logic Toolbox

The FIS Editor handles the high level issues for the system: How much input and output variables? What are their names? The Fuzzy Logic Toolbox doesn't limit the number of inputs. However, the number of inputs may be limited by the available memory of your machine. If the number of inputs is too large, or the number of membership functions is too big, then it may also be difficult to analyze the FIS using the other GUI tools. The Membership Function Editor is used to define the shapes of all the membership functions associated with each variable. The Rule Editor is for editing the list of rules that defines the behaviour of the system.

	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NB	NM	NS	ZE	PS
NS	NB	NB	NM	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PM	PB	PB
PM	NS	ZE	PS	PM	PB	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

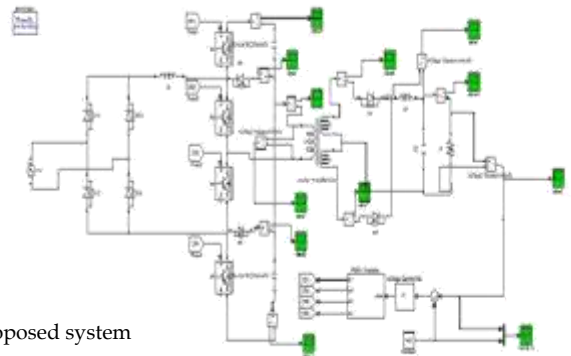


Fig 6. The Simulink model of Proposed system

## VI.SIMULATION RESULTS AND DISCUSSIONS:

A 500 W/48 V simulation has been designed to serve as the proof of concept, as shown in Fig. 6. Two split capacitors each one rated at 470  $\mu$ F/400 V are connected to the dc-link. The output capacitor is 100  $\mu$ F. The input and output inductors are chosen as 27  $\mu$ H/15 A. Two identical input inductors are connected in parallel (one of them is mounted on the bottom side of the pcb), which is equivalent to 13.5  $\mu$ H/30 A. The switching frequency of the switches is set to 125 kHz. The transformer core is ETD-49, manufactured by EPCOS. The turns ratio of the transformer is 1:2. The neutral point clamping diodes (D5 and D6 ) are Cree SiC diodes, which are rated at 600 V/ 16.5 A. The diode rectifier, manufactured by Diodes Inc., is rated at 600 V/15 A. The power switches (S1 to S4 ) are N Channel MOSFETs, which are rated at 400 V/25 A. The output rectification diodes (D7

and D8 ) are rated at 200 V/30 A.

The converter is air-cooled with external fans. The switching pattern is given in Fig. 6. The experimental waveforms of input voltage, input current and dc-link voltage are given in Fig.5. The input power is 480 W for this case. The ac voltage is supplied from an ac power source at 90 Vrms at 60 Hz. The input inductor current is discontinuous, and S2 - S3 switch pair is switched at constant duty cycle. It is worth mentioning that an LC network, connected to the circuit externally, is employed to filter the input current. The filtered input current is presented in Fig. 9. The high PF can be observed from the alignment of input voltage and current, and the sinusoidal envelope. DC-link voltage slightly oscillates with the twice of the input frequency around 400 V. For the test condition of  $V_{in} = 90\text{ V}$  and  $V_{dc} = 400\text{ V}$ , the THDs for 100% and 50% loads are recorded as 7.02% and 9.71%, respectively.

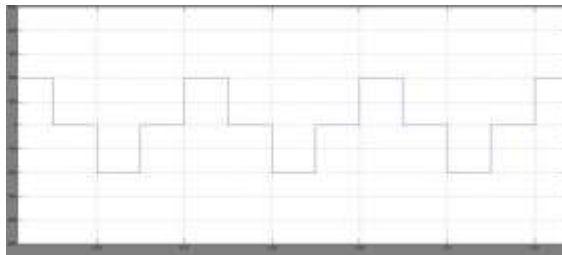


Fig 7 Primary Transformer Voltage

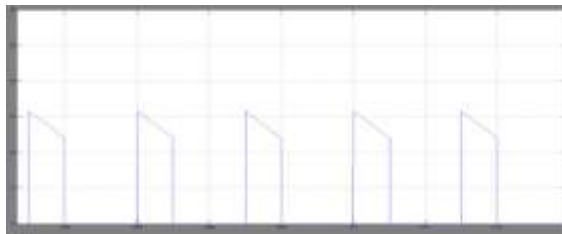
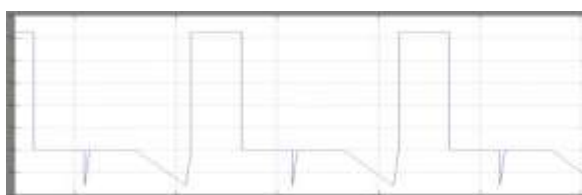


Fig 8 Diode Current ( $I_{d6}$ )



Fig 9 Capacitor Current( $I_{dc2}$ )



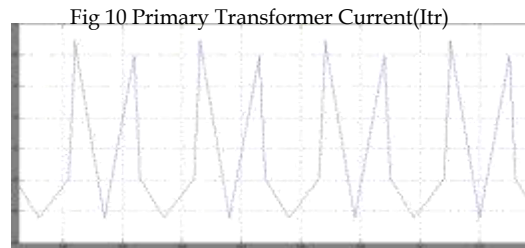


Fig 11 Capacitor Current (I<sub>dc1</sub>)

The input current ripple frequency is twice of the switching frequency contributing to using smaller PFC inductor. Two independent controllers, in favour of shaping the input current and regulating the output voltage, are adopted which simplifies the design and control of the circuit. The tradeoff between the PF and overall efficiency in the case of adopting a variable dc-link voltage is analysed through developed loss model. The results of the analyses show that under 265 V line voltages, the PF can be increased to 0.99 from 0.88 by varying the dc-link voltage from 400 to 800 V. On the other hand, the efficiency of an 800 W/48 V converter can drop from 95.2% to 90% at full load. A fuzzy controlled three-level isolated single stage PFC converter is designed and simulated in MATLAB/SIMULINK. A high PF of .99 and output voltage regulation (48 V) is achieved. A sinusoidal input current wave shape is also obtained. The response of the converter is faster. Output voltage and current ripples are minimum. The controller uses minimum number of components compared to other PF converters.

## CONCLUSION

In this paper, a three-level single-stage PFC ac/dc converter is proposed for low-power applications. The proposed converter exhibits high PF with less number of switches/diodes, operated at constant duty ratio. A PFC inductor and a diode bridge are added to the conventional three-level isolated dc/dc converter, while the switching scheme

## REFERENCES

- [1] J. R. Morrison and M. G. Egan, "A new modulation strategy for a buckboost input AC/DC converter," *IEEE Trans. Power Electron.*, vol. 16, no. 1, pp. 34–45, Jan. 2001.
- [2] H. Wang, S. Dusmez, and A. Khaligh, "Design and analysis of a full bridge LLC based PEV charger optimized for wide battery voltage range," *IEEE Trans. Veh. Technol.*, vol. 63, no. 4, pp. 1603–1613, May 2014.
- [3] J. Y. Lee and H. J. Chae, "6.6-kW on-board charger design using DCM PFC converter with harmonic modulation technique and two-stage DC/DC converter," *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1243–1252, Mar. 2014.
- [4] A. Khaligh and S. Dusmez, "Comprehensive topological analyses of conductive and inductive charging solutions for plug-In electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 61, no. 8, pp. 3475–3489, Oct. 2012.
- [5] H. Ma, Y. Ji, and Y. Xu, "Design and analysis of single-stage power factor correction converter with a feedback winding," *IEEE Trans. Power Electron.*, vol. 25, no. 6, pp. 1460–1470, Jun. 2010.