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HIGH RELIABILITY AND EFFICIENCY OF GRID-CONNECTED PHOTOVOLTAIC SYSTEMS USING SINGLE-PHASETRANSFORMERLESS INVERTER

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Abstract

This paper presents a high-reliability single- phase transformerless grid-connected inverter that utilizes super junction MOSFETs to achieve high efficiency for photovoltaic applications. The proposed converter utilizes two split ac-coupled inductors that operate separately for positive and negative half grid cycles. This eliminates the shoot-through issue that is encountered by traditional voltage source inverters, leading to enhanced system reliability. Dead time is not required at both the high- frequency pulse width modulation switching commutation and the grid zero-crossing instants, improving the quality of the output ac-current and increasing the converter efficiency. The split structure of the proposed inverter does not lead itself to the reverse-recovery issues for the main power switches and as such super junction MOSFETs can be utilized without any reliability or efficiency penalties. Since MOSFETs are utilized in the proposed converter high efficiency can be achieved even at light load operations achieving a high California energy commission (CEC) or European Union efficiency of the converter system. It also has the ability to operate at higher switching frequencies while maintaining high efficiency. The higher operating frequencies with high efficiency enables reduced cooling requirements and results in system cost savings by shrinking passive components. With two additional ac-side switches conducting the currents during the freewheeling phases, the photovoltaic array is decoupled from the grid. This reduces the high-frequency common-mode voltage leading to minimized ground loop leakage current. The operation principle, common-mode characteristic and design considerations of the proposed transformerless inverter are illustrated. The total losses of the power semiconductor devices of several existing transformerless inverters which utilize MOSFETs as main switches are evaluated and compared. The experimental results with a 5 kW prototype circuit show 99.0% CEC efficiency and 99.3% peak efficiency with a 20 kHz switching frequency. The high reliability and efficiency of the proposed converter makes it very attractive for single-phase transformerless photovoltaic inverter applications.

Index Terms—**California energy commission (CEC) efficiency, European Union (EU) efficiency, MOSFET inverters, high efficiency, high reliability, transformerless grid-connected photo-voltaic inverter.**

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I. INTRODUCTION

TRANSFORMERLESS photovoltaic (PV) grid-connected inverters have the advantages of higher efficiency, lower cost, less complexity, and smaller volume compared to their counterparts with transformer galvanic isolation. High- frequency common-mode (CM) voltages must be avoided for a transformerless PV grid-connected inverter because it will lead to a large charge/discharge current partially flowing through the inverter to the ground. This CM ground current will cause an increase in the current harmonics, higher losses, safety problems, and electromagnetic interference (EMI) issues. For a grid-connected PV system, energy yield and payback time are greatly dependant on the inverter's reliability and efficiency, which are regarded as two of the most significant characteristics for PV inverters. In order to minimize the ground leakage current and improve the efficiency of the converter system, transformerless PV inverters utilizing unipolar PWM control have been presented .The weighted California Energy Commission (CEC) or European Union (EU) efficiencies of most commercially available and literature-reported single-phase PV transformerless inverters are in the range of 96–98%. Recently, several transformerless inverter topologies have been presented that use super junction MOSFETs devices as main switches to avoid the fixed voltage-drop and the tail-current induced turn-off losses of IGBTs to achieve ultra high efficiency (over 98% weighted efficiency).

One commercialized unipolar inverter topology, H5, as shown in Fig. 1(a), solves the ground leakage current issue and uses hybrid MOSFET and IGBT devices to achieve high efficiency. The reported system peak and CEC efficiencies with an 8-kW converter system from the product datasheet is 98.3% and 98%, respectively, with 345-V dc input voltage and a 16-kHz switching frequency. However, this topology has high conduction losses due to the fact that the current must conduct through three switches in series during the active phase. Another disadvantage of the H5 is that the line-frequency switches S1 and S2 cannot utilize MOSFET devices because of the MOSFET body diode's slow reverse recovery. The slow reverse recovery of the MOSFET body diode can induce large turn-on losses, has a higher possibility of damage to the devices and leads to EMI problems. Shoot-through issues associated with traditional full bridge PWM inverters remain in the H5 topology due to the fact that the three active switches are series-connected to the dc bus.

Replacing the switch S5 of the H5 inverter with two split switches S5 and S6 into two phase legs and adding two free-wheeling diodes D5 and D6 for freewheeling current flows, the H6 topology was proposed in The H6 inverter can be implemented using MOSFETs for the line frequency switching devices, eliminating the use of less efficient IGBTs. The reported peak efficiency and EU efficiency of a 300 W proto- type circuit were 98.3% and 98.1%, respectively, with 180 V dc input voltage and 30 kHz switching frequency. The fixed- voltage conduction losses of the IGBTs used in the H5 inverter are avoided in the H6 inverter topology improving efficiency; however, there are higher conduction losses due to the three series-connected switches in the current path during active phases. The shoot-through issues due to three active switches series connected to the dc-bus still remain in the H6 topology. Another disadvantage to the H6 inverter is that when the inverter output voltage and current has a phase shift the MOSFET body diodes may be activated. This can cause body diode reverse-recovery issues and decrease the reliability of the system.

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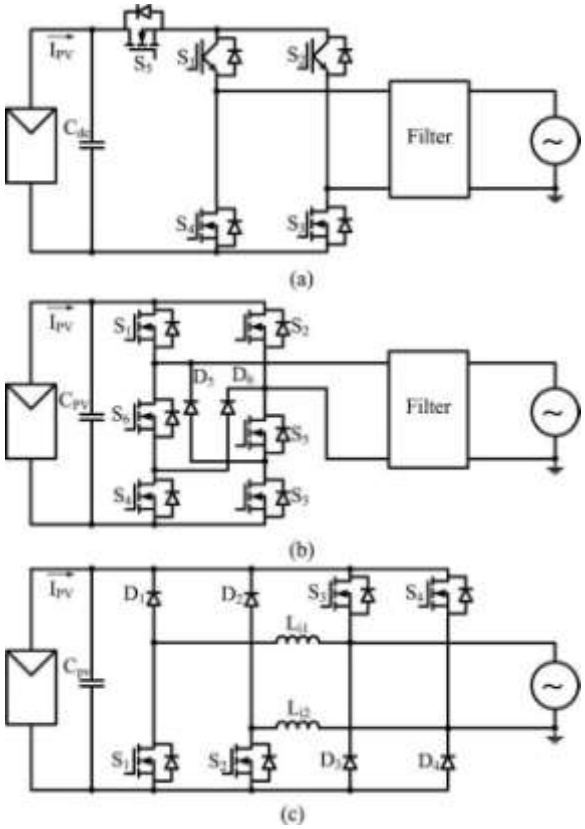

Fig. 1. Single-phase transformerless PV inverters using super junction MOSFETs: (a) H5, (b) H6, and (c) dual-paralleled-buck inverters.

Another high-efficiency transformerless MOSFET inverter topology is the dual-paralleled-buck converter, as shown in Fig. 1(c). The dual-parallel-buck converter was inversely de- rived from the dual-boost bridgeless power-factor correction (PFC) circuit in. The dual-paralleled-buck inverter eliminates the problem of high conduction losses in the H5 and H6 Inverter topologies because there are only two active switches in series with the current path during active phases. The reported maximum and EU efficiencies of the dual-paralleled- buck inverter using Cool MOS switches and SiC diodes tested on a 4.5 kW prototype circuit were 99% and 98.8%, respectively, with an input voltage of 375 V and a switching frequency at 16 kHz. The main issue of this topology is that the grid is directly connected by two active switches S3 and S4, which may cause a grid short-circuit problem, reducing the reliability of the topology. A dead time of 500μs between the line-frequency switches S3 and S4 at the zero-crossing instants needed to be added to avoid grid shoot-through. This adjustment to improve the system reliability comes at the cost of high zero-crossing distortion for the output grid current. One key issue for a high efficiency and reliability transformer- less PV inverter is that in order to achieve high efficiency over a wide load range it is necessary to utilize MOSFETs for all switching devices. Another key issue is that the inverter should not have any shoot-through issues for higher reliability.

In order to address these two key issues, a new inverter topology is proposed for single-phase

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transformerless PV grid-connected systems in this paper. The proposed transformerless PV inverter features: 1) high reliability because there are no shoot-through issues, 2) low output ac current distortion as a result of no dead- time requirements at every PWM switching commutation instant as well as at grid zero-crossing instants, 3) minimized CM leakage current because there are two additional ac-side switches that decouple the PV array from the grid during the freewheeling phases, and 4) all the active switches of the pro-posed converter can reliably employ super junction MOSFETs since it never has the chance to induce MOSFET body diode reverse recovery. As a result of the low conduction and switching losses of the super junction MOSFETs, the proposed converter can be designed to operate at higher switching frequencies while maintaining high system efficiency. Higher switching frequencies reduce the ac- current ripple and the size of passive components. Detailed power stage operation principle, PWM scheme, and CM leakage current analysis are described in this paper. The total losses of power devices for several existing MOS- FET inverters are comparatively evaluated. The loss reduction by replacing IGBTs with super junction MOSFETs as power switches for the proposed transformerless inverter is analyzed. To verify the effectiveness and demonstrate the performance of the proposed transformerless inverter, a 5 kW prototype circuit was built and tested using two different switching frequencies, 20 and 40 kHz. Experimental results show that the proposed inverter topology not only eliminates the issues of MOSFET body diode reverse recovery, ground leakage current, and shoot-through; it also achieves 99.3% maximum efficiency and 99.0% CEC efficiency with high-quality output current waveforms.

II. PROPOSED TOPOLOGY AND OPERATION ANALYSIS

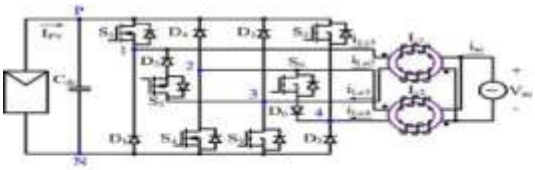
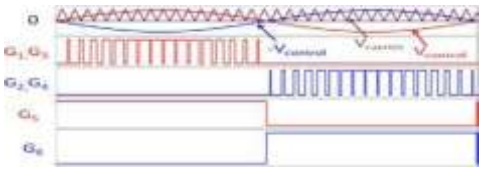


Fig. 2. Proposed high efficiency and reliabil



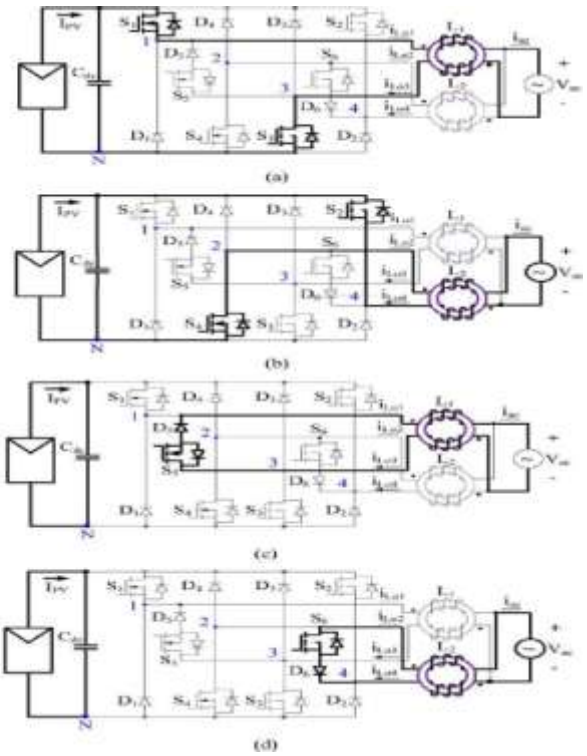


Fig. 2 shows the circuit diagram of the proposed transformerlss PV inverter, which is composed of

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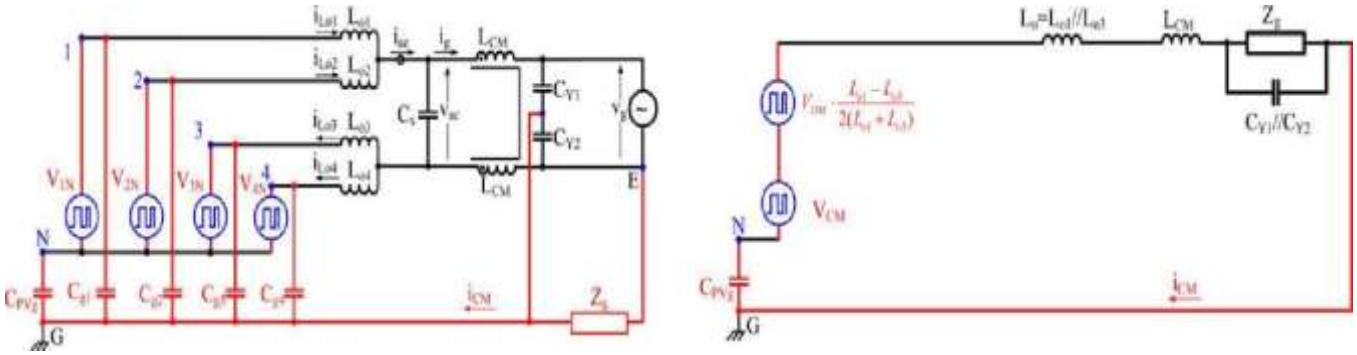
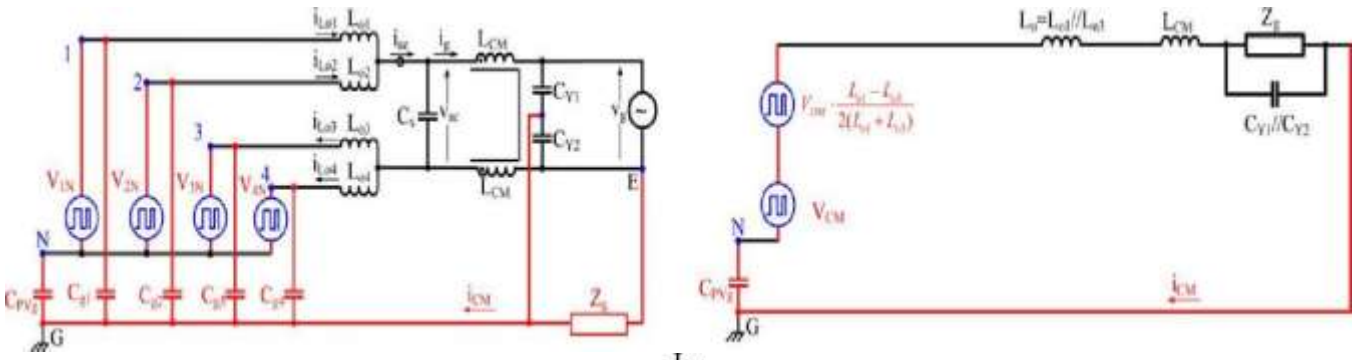
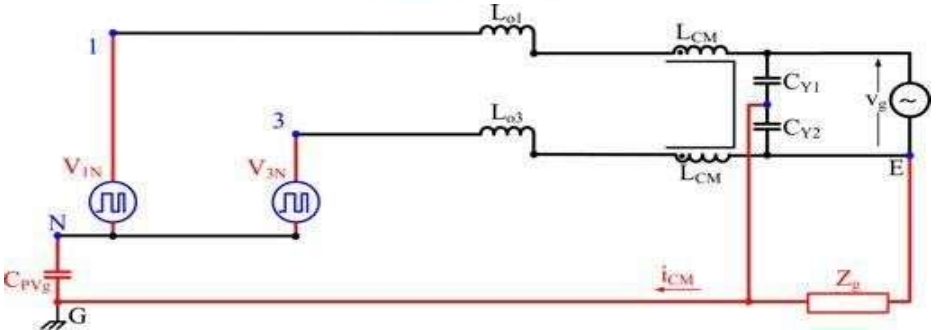
six MOSFETs side switch pairs are composed of respectively, which provide unidirectional current flow branches during the freewheeling phases decoupling the grid from the PV array and minimizing the CM leakage current. Compared to the HERIC topology the proposed inverter topology divides the ac side into two in-dependent units for positive and negative half cycle. In addition to the high efficiency and low leakage current features, the proposed transformerless inverter avoids shoot- through enhancing the reliability of the inverter. The inherent structure of the proposed inverter does not lead itself to the reverse recovery issues for the main power switches and as such super junction MOSFETs can be utilized without any reliability or efficiency penalties Fig. 3 illustrates the PWM scheme for the proposed inverter. When the reference signal $V_{control}$ is higher than zero, MOS- FETs S1 and S3 are switched simultaneously in the PWM mode and S5 is kept on as a polarity selection switch in the half grid cycle; the gating signals G2 , G4 , and G6 are low and S2 , S4 , and S6 are inactive. Similarly, if the reference signal – $V_{control}$ is higher than zero, MOSFETs S2 and S4 are switched simultaneously in the PWM mode and S6 is on as a polarity selection switch in the grid cycle; the gating signals G1 , G3 , and G5 are low and S1 , S3 , and S5 are inactive. Fig. 4 shows the four operation stages of the proposed inverter within one grid cycle. In the positive half-line grid cycle, the high-frequency switches S1 and S3 are modulated by the sinusoidal reference signal $V_{control}$ while S5 remains turned ON.







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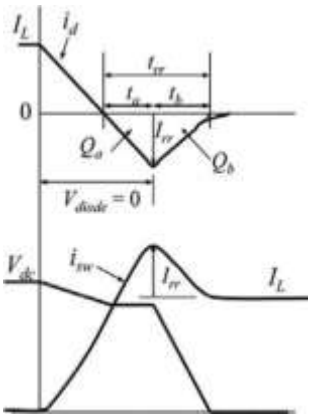

Fig. 8. Simplified waveforms showing switching losses induced in the main switches and diodes during diode reverse recovery.

TABLE I
TOTAL LOSSES OF POWER DEVICES AT DIFFERENT CEC OUTPUT POWER CONDITIONS AT 20 KHZ SWITCHING FREQUENCY

Po (%)	H5 (W)	H6 (W)	DPB (W)	Proposed (W)
100%	76.99	68.65	53.56	53.56
75%	41.24	43.04	34.55	34.55
50%	30.67	23.89	20.12	20.12
30%	17.92	13.23	11.87	11.87
20%	12.79	9.45	8.85	8.85
10%	8.48	7.80	6.56	6.56

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The third part of the switching losses is the switching loss induced in the diode during the diode reverse recovery interval, which can be approximated as

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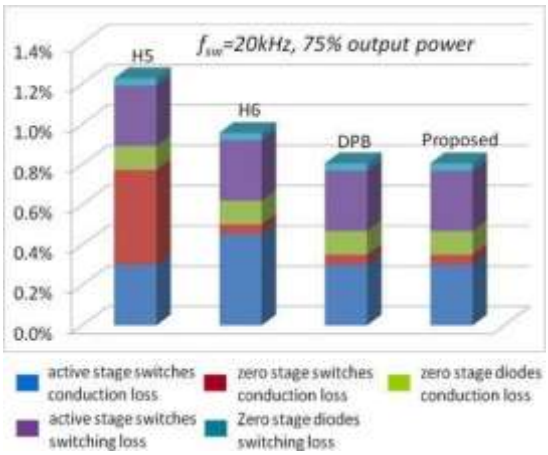
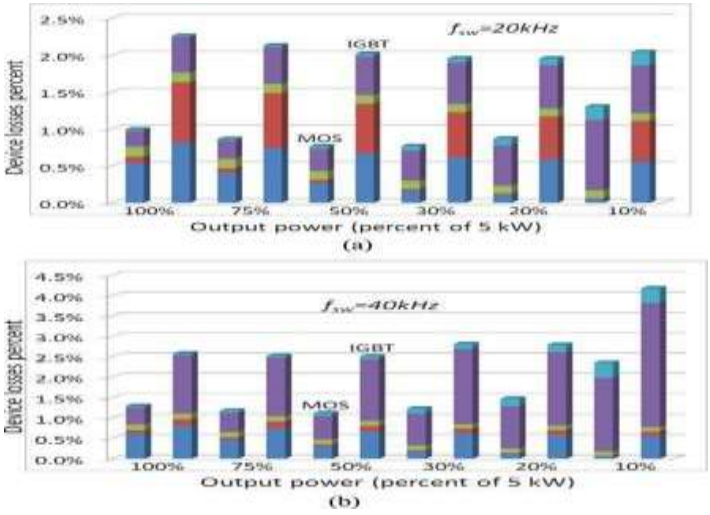


Fig. 9. Power semiconductor device losses distribution comparison for H5, H6, DPB, and proposed transformerless PV inverters with 75% of the rated output power.

The power semiconductor device losses distribution for H5, H6, DPB, and proposed inverters at 75% of the rated output power condition, which is the most dominant term in CEC efficiency evaluation, is also shown in Fig. 9. It can be seen from Fig. 9 that the switching losses for these four MOSFET inverters are almost the same. The conduction losses of H5 are highest because of the IGBT's fixed voltage drop. The conduction losses of the H6 inverter are higher than DPB and the proposed inverters because one more switch is in series in the current path during the active stages. The proposed transformer- less inverter can achieve the same high efficiency as the DPB MOSFET inverter in. However, the reliability of the pro- posed converter is greatly enhanced and the quality of output ac current is improved compared to the DPB MOSFET inverter

in [13].



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The power semiconductor device losses distribution for the proposed inverter with MOSFETs and IGBTs at different CEC output power with operating switching frequencies of 20 and 40 kHz are comparatively illustrated in Fig. 10(a) and (b), respectively. From Fig. 10(b), when IGBTs are employed as power devices, the total power semiconductor device losses of the proposed inverter are already more than 2.4% for all tested power ranges in CEC efficiency calculation at 40 kHz switching frequency. If other losses such as output inductor loss, gate drive loss, and control board loss are included, the losses of the whole inverter system will be above 3%. As a result, the efficiency of the whole inverter system is less than 97%, which is relatively low for a transformerless grid-connected PV inverter. On the other hand, for the MOSFET inverter operating at 40 kHz switching frequency, the total power semiconductor device losses are less than 1.2% with the output power higher than 30% of the rated power and no more than 2.4% even at 10% output power.

SPECIFICATIONS AND POWER STAGE DEVICES FOR PROTOTYPE CIRCUIT

Nominal input voltage	380V
Grid voltage	240Vac
Nominal frequency	60Hz
Nominal output power	5 kW
Nominal AC current	21A
S_1~S_6	IPW60R041C6, $R_{ds\,(on),max}$= 41mΩ
D_1~D_6	APT30DQ60BG
L_1,L_2	0.95mH
C_f	2.2uF
Lg	0.25mH
Cx	0.15uF
Lcm	17.65mH
C_{Y1},C_{Y2}	2.2nF
C_{PVg}	100nF
Digital Controller	Texas Instrument's 28335

Hence, a higher switching frequency operation can be adopted for the proposed inverter with super junction MOSFETs to reduce the output current rip- ple and the size of passive components, while the inverter still maintains an high-level system efficiency.

III. EXPERIMENTAL VERIFICATIONS

A 5 kW prototype circuit has been designed, fabricated, and tested to verify the performance of the proposed transformerless PV inverter topology. Fig. 11 describes the block diagram of the complete grid-connected inverter test system. G_i (s) is a quasi-proportional- resonant current controller and G_C (s) is an admittance compensator [37]. Specifications of the inverter and the selection of power stage devices are shown in Table III. The photograph of the test-bed hardware prototype is shown in Fig. 12.

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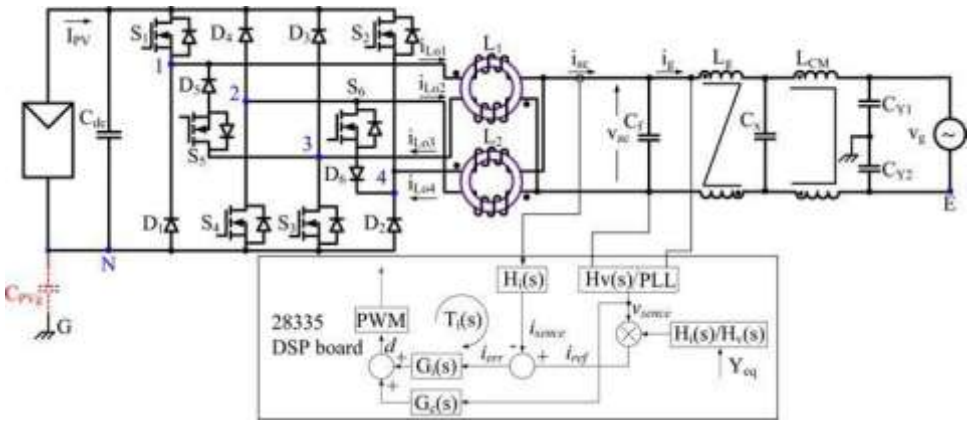
The experimental gating signals in the grid cycle and in the PWM cycle are shown in Fig. 13(a) and (b), respectively. It can be seen that the experimental gating signals G1 , G3 , and G5 agree with the analysis results of the PWM scheme and the gating signals of G1 and G3 are synchronized well. The drain–source voltage waveforms of the switches S1 , S3 , and S5 in the grid cycle and in the PWM cycle are shown in Fig. 14(a) and (b), respectively. The voltage stresses of S1 , S3 , and S5 are well clamped to the dc bus voltage, 380 V, without any voltage overstress. It can be seen from Fig. 14(b) that the switches S1 and S3 almost evenly share the dc-link voltage when they switch OFF simultaneously; effectively minimizing the ground loop leakage current Fig. 15 shows the experimental waveforms of the ground potential V_{EN} . It can be seen that the high-ground leakage current is avoided because the high-frequency voltage of the ground potential is eliminated at every PWM switching commutation and at zero-crossing instants.



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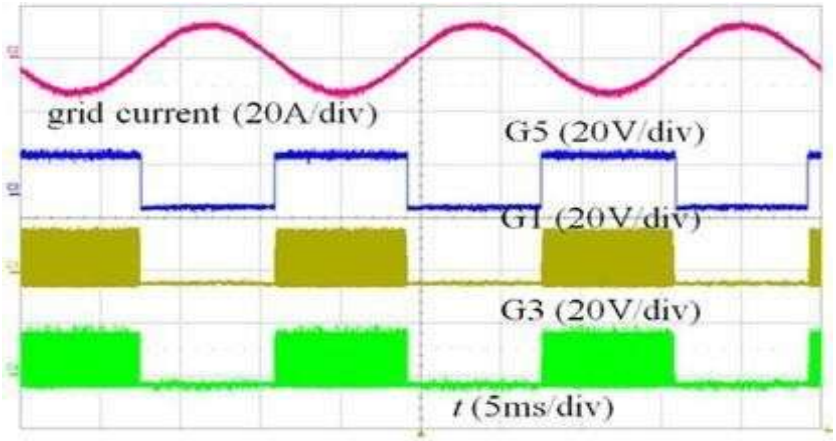
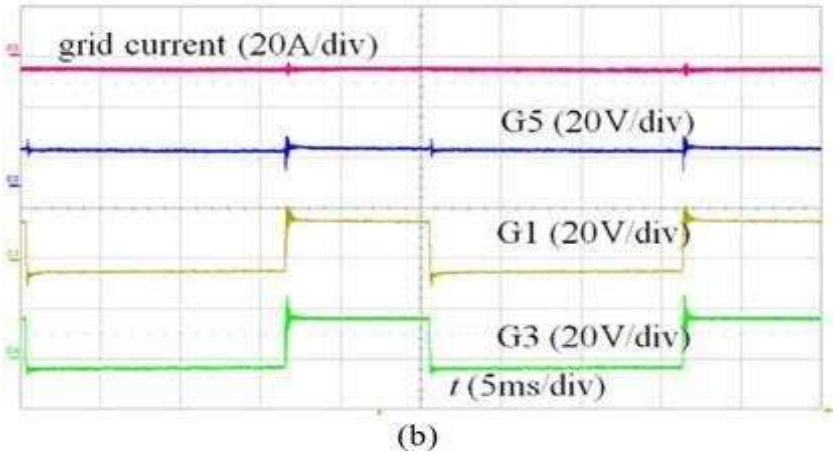
The experimental waveforms of the grid current i_g , the inductor currents i_{Lo1} , and i_{Lo2} under the 240 Vrm s grid voltage and half-load conditions are shown in Fig. 16. This figure shows that the proposed inverter presents high-power factor and low-harmonic distortion Fig. 17 shows the leakage current test waveforms, the CM leakage current is successfully limited with the peak value 59.5 mA and rms value 10.33 mA, which are well below the limitation requirements of the German standard VDE0126-1-1 Fig. 18 shows the measured efficiencies as a function of the output power for the proposed transformerless PV inverter at switching frequencies of 20 and 40 kHz. Note that the presented efficiency diagram covers the losses of the main power stage including power semiconductor device losses and output inductor losses, but it does not include the power consumption of control circuit and the associated driver circuit.



(a)



(b)

The calculated CEC efficiencies of the proposed transformer- less inverter at 20 and 40 kHz switching frequencies are 99% and 98.8%, respectively. The CEC efficiency at 40 kHz switch-ing frequency is about 0.2% lower than at 20 kHz switching frequency operation. However, 40 kHz operation can gain the benefits of reduced output current ripple and the reduced size of passive components.

CONCLUSION

A high reliability and efficiency inverter for transformerless PV grid-connected power generation systems is presented in this paper. The main characteristics of the proposed transformerless inverter are summarized as follows:

1) ultra high efficiency can be achieved over a wide output power range by reliably employing superjunction MOS- FETs for all switches since their body diodes are never activated;
2) no shoot-through issue leads to greatly enhanced reliabil-ity;
3) low ac output current distortion is achieved because dead time is not needed at PWM switching commutation in-stants and grid-cycle zero-crossing instants;
4) low-ground loop CM leakage current is present as a result of two additional unidirectional-current switches decou- pling the PV array from the grid during the zero stages;
5) higher switching frequency operation is allowed to reduce the output current ripple and the size of passive compo- nents while the inverter still maintains high efficiency;
6) the higher operating frequencies with high efficiency en- ables reduced cooling requirements and results in system cost savings by shrinking passive components.

The experimental results tested on a 5 kW hardware prototype verify the effectiveness of the proposed converter and show 99.0% CEC efficiency. With the super high efficiency, low- leakage ground loop CM current, high quality of output current and greatly enhanced reliability, the proposed topology is very attractive for transformerless PV inverter applications.

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